Carbon Nanotube Electronics

PHAEDON AVOURIS, MEMBER, IEEE, JOERG APPENZELLER, RICHARD MARTEL, AND SHALOM J. WIND, SENIOR MEMBER, IEEE

Invited Paper

We evaluate the potential of carbon nanotubes (CNTs) as the basis for a new nanoelectronic technology. After briefly reviewing the electronic structure and transport properties of CNTs, we discuss the fabrication of CNT field-effect transistors (CNTFETs) formed from individual single-walled nanotubes (SWCNTs), SWCNT bundles, or multiwalled (MW) CNTs. The performance characteristics of the CNTFETs are discussed and compared to those of corresponding silicon devices. We show that CNTFETs are very competitive with state-of-the-art conventional devices. We also discuss the switching mechanism of CNTFETs and show that it involves the modulation by the gate field of Schottky barriers at the metal-CNT junctions. This switching mechanism can account for the observed subthreshold and vertical scaling behavior of CNTFETs, as well as their sensitivity to atmospheric oxygen. The potential for integration of CNT devices is demonstrated by fabricating a logic gate along a single nanotube molecule. Finally, we discuss our efforts to grow CNTs locally and selectively, and a method is presented for growing oriented SWCNTs without the involvement of a metal catalyst.

Keywords*—*Carbon nanotubes (CNTs), field-effect transistors (FETs), molecular electronics, nanoelectronics.

I. INTRODUCTION

Carbon nanotubes (CNTs) are hollow cylinders composed of one or more concentric layers of carbon atoms in a honeycomb lattice arrangement. Multiwalled nanotubes (MWCNTs) were observed for the first time in transmission electron microscopy (TEM) studies by Iijima in 1991 [1], while single-walled nanotubes (SWCNTs) were produced independently by Iijima [2] and Bethune [3] in 1993.

SWCNTs typically have a diameter of 1–2 nm and a length of several micrometers. The large aspect ratio makes the nanotubes nearly ideal one-dimensional (1-D) objects, and as such the SWCNTs are expected to have all the unique properties predicted for these low-dimensional structures [4]–[7]. In addition, as we discuss below, depending on the detailed arrangement of the carbon atoms the SWCNTs can be metallic or semiconducting [8], [9]. Furthermore, the C–C bonds in CNTs are very strong, resulting in an extremely high mechanical stability (Young's modulus about ten times higher than that of steel) and chemical inertness. The strong, covalent bonding also leads to near perfect side-wall structures with very few defects.

CNTs are currently considered as promising building blocks of a future nanoelectronic technology. This is not simply due to their small size but rather to their overall properties. In fact, many of the problems that silicon technology is or will be facing are not present in CNTs. Below we list some of these CNT properties and their implications for electronics.

1) Carrier transport is 1-D. This implies a reduced phase space for scattering of the carriers and opens up the possibility of ballistic transport. Correspondingly, power dissipation is low. Furthermore, as we discuss in Section II, their electrostatic behavior is different from that of silicon devices with implications on screening and electron/hole tunneling.
2) All chemical bonds of the C atoms are satisfied and there is no need for chemical passivation of dangling bonds as in silicon. This implies that CNT electronics would not be bound to use SiO_2 as an insulator. High dielectric constant and crystalline insulators can be used, allowing, among other things, the fabrication of three-dimensional (3-D) structures.
3) The strong covalent bonding gives the CNTs high mechanical and thermal stability and resistance to electromigration. Current densities as high as 10^9 A/cm^2 can be sustained [10].
4) Their key dimension, their diameter, is controlled by chemistry, not conventional fabrication.
5) In principle, both active devices (transistors) and interconnects can be made out of semiconducting and metallic nanotubes, respectively.

We see that the properties of the SWCNTs are truly remarkable. However, finding ways to effectively exploit these properties remains a challenge. In the rest of this paper

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The authors are with the IBM Research Division, T. J. Watson Research Center, Yorktown Heights, NY 10598 USA (e-mail: avouris@us.ibm.com).

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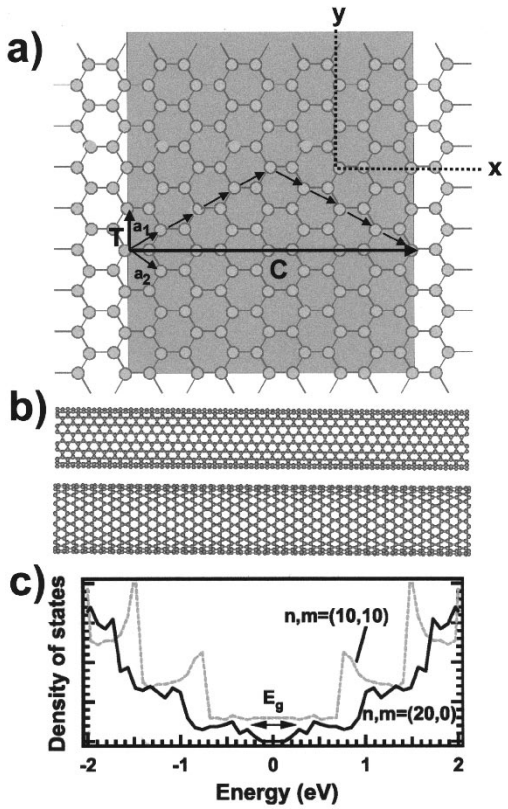

Fig. 1. (a) Description of the structure of CNTs in terms of the chirality vector **C** and the (n,m) indices. The example shown involves a (4,4) tube. (b) Atomic structure of a metallic (10,10) CNT (top) and a semiconducting (20,0) CNT (bottom), and (c) the corresponding density of states versus energy plots.

we will review the electronic structure of the CNTs and then present our efforts to fabricate nanotube transistors and simple integrated circuits and understand the underlying device physics.

II. Electronic Structure of Carbon Nanotubes

The electronic structure and electrical properties of SWCNTs are usually discussed in terms of the electronic structure of a graphene sheet (a layer of graphite) [4]–[9]. The SWCNT can be thought of as being formed by folding a piece of graphene to give a seamless cylinder. The circumference of the nanotube is expressed by the so-called chirality vector, $\mathbf{C}$, connecting two crystallographically equivalent sites of the two-dimensional (2-D) graphene sheet (see Fig. 1). $\mathbf{C} = n\mathbf{a}_1 + m\mathbf{a}_2$, where $\mathbf{a}_1$ and $\mathbf{a}_2$ are the unit vectors of the hexagonal honeycomb lattice, so that any nanotube can be described by a pair of integers (n,m) that define its chiral vector. For example, the chiral vector shown in Fig. 1(a) describes a (4,4) nanotube. The unit shell of the nanotube is defined as the rectangle formed by $\mathbf{C}$ and the 1-D translational vector $\mathbf{T}$ identified in Fig. 1. Also shown are the atomic structures of a (10,10) and a (20,0) CNT [Fig. 1(b)] and their density of states [Fig. 1(c)].

The interesting electrical properties of CNTs are due in a large part to the peculiar electronic structure of the graphene. Its band structure and its hexagonal first Brillouin zone

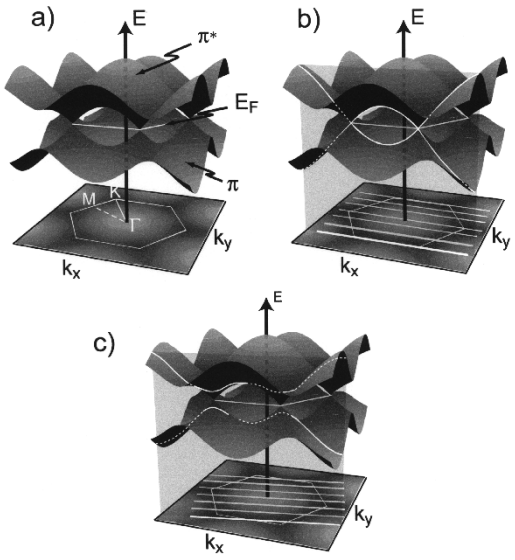

Fig. 2. (a). Band structure of a graphene sheet (top) and the first Brillouin zone (bottom). (b) Band structure of a metallic (3,3) CNT. (c) Band structure of a (4,2) semiconducting CNT. The allowed states in the nanotubes are cuts of the graphene bands indicated by the white lines. If the cut passes through a K point, the CNT is metallic; otherwise, the CNT is semiconducting.

are shown in Fig. 2(a). The energy surfaces describing the valence (π) and conduction (π^*) states touch at six points (Fermi points) lying at the Fermi level. This unusual band structure has immediate consequences for the electronic properties of graphene. While allowed states exist at the Fermi level, the dimensionality of the system (2-D) results in a vanishing density of states when integrating over the Fermi surface. Because of this particular situation, graphene is a zero-gap semiconductor.

In the case of a nanotube there is an additional quantization arising from the confinement of the electrons in the circumferential direction in the tube. This requires that the circumferential component of the wave vector $\boldsymbol{k}_C$ can only take the values fulfilling the condition $\boldsymbol{k}_C \cdot \mathbf{C} = 2\pi j$ where $\mathbf{C}$ is again the chirality vector and j an integer. As a result, each band of graphene splits into a number of 1-D subbands labeled by j. Fig. 2(b) shows the states of a (3,3) CNT. The allowed energy states of the tube are cuts of the graphene band structure. When these cuts pass through a Fermi point, as in the case of the (3,3) nanotube, the tube is metallic. In cases where no cut passes through a K point, the tubes are semiconducting [Fig. 2(c)]. It can be shown that an (n,m) CNT is metallic when $n = m$, it has a small gap (due to curvature-induced $\sigma - \pi$ mixing) when $n - m = 3i$ [11], where i is an integer, while CNTs with $n - m \neq 3i$ are truly semiconducting [8], [9].

As long as we restrict our interest to low energies (i.e., a few hundred meV from the Fermi energy E_F) the band structure of a metallic nanotube can be approximated by two sets of bands with a linear dispersion intersecting at k_F and $-k_F$ [see white lines in Fig. 2(b)]. Electrons with dE/dk > 0 move to the right, while electrons with dE/dk < 0 move to the left. In semiconducting CNTs the two bands do not cross at E_F, but a diameter-dependent band gap develops

with $E_{\mathrm{GAP}} = (4\hbar v_F/3d_{\mathrm{CNT}})$, where d_{CNT} is the tube's diameter and v_F the Fermi velocity [8], [9]. The above theoretical predictions have been confirmed experimentally by scanning tunneling spectroscopy [12], [13].

The SWCNTs are 1-D objects and as such their two-terminal conductance is given by Landauer's equation: [14], [15] $G = (2e^2/h) \cdot \sum_i^N T_i$ where $2e^2/h$ is the quantum of conductance and T_i is the transmission of a contributing conduction channel (subband). The sum involves all contributing conduction channels, i.e., channels whose energy lies between the electrochemical potentials of the left and right reservoirs to which the nanotube is connected. In the absence of any scattering, i.e., when all $T_i = 1$, the resistance $(R = 1/G)$ of a metallic SWCNT is $h/(4e^2) \approx 6.5\ \mathrm{k}\Omega$ because, as we discussed above, $N = 2$. This quantum mechanical resistance is a contact resistance arising from the mismatch of the number of conduction channels in the CNT and the macroscopic metal leads.

There is strong evidence that $T\lambda 1$ in the case of metallic SWCNTs, so that these tubes behave as ballistic conductors [16]–[19]. This arises from the 1-D confinement of the electrons which allows motion in only two directions. This constraint along with the requirements for energy and momentum conservation severely reduces the phase space for scattering processes. However, in addition to the quantum mechanical contact resistance, there are other sources of contact resistance, such as those produced by the existence of metal-nanotube interface barriers, or poor coupling between the CNT and the leads. These types of resistance are very important and can dominate electrical transport in nanotubes, especially at low temperatures where typically they lead to charging and the observation of Coulomb blockade phenomena. Localization can also be induced by contacts to metallic electrodes, a fact that makes four-probe measurements very difficult, requiring special arrangements [19].

Unlike SWCNTs, the electrical properties of MWCNTs have received less attention. This is due to their complex structure; every carbon shell can have different electronic character and chirality, and the presence of shell–shell interactions [20], [21]. However, at low bias and temperatures, and when MWCNTs are side-bonded to metallic electrodes, transport is dominated by outer-shell conduction [10], [22], [23]. MWCNTs show 1-D or 2-D characteristics, depending on their diameter and the property considered.

III. Fabrication and Performance of Carbon Nanotube FETs

FETs, particularly in CMOS form, have been proven to be the most technologically useful device structures. It is, thus, natural that we have chosen to build such devices using CNTs. The first such devices were fabricated in 1998 [24], [25]. In these a single SWCNT was used to bridge two noble metal electrodes prefabricated by lithography on an oxidized silicon wafer as shown in Fig. 3. The SWCNT played the role of the "channel," while the two metal electrodes functioned as the "source" and "drain" electrodes. The heavily

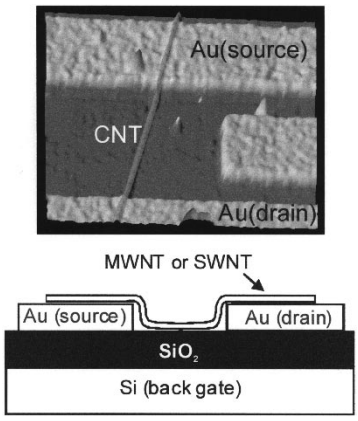

Fig. 3. Top: AFM image of one of our early CNTFETs. Bottom: Schematic cross section of the CNTFET [25].

doped silicon wafer itself was used as the "gate" (back-gate). These CNTFETs behaved as p-type FETs (we will return to this point in Section V) and had an I(on)/I(off) current ratio of $\approx 10^5$. While functional, the devices had a high parasitic contact resistance $(\geq 1\ \mathrm{M}\Omega)$, low drive currents (a few nanoamperes), low transconductance $g_m \sim 1$ nS, and high inverse subthreshold slopes S$\sim$1–2 V/decade. To a large extent the unsatisfactory characteristics were due to bad contacts. The CNT was simply laid on the gold electrodes and was held by weak van der Waals forces. To improve the contacts we adapted a different fabrication scheme where the semiconducting SWCNTs (s-SWCNTs) were dispersed on an oxidized Si wafer, and the source and drain electrodes, now made of metals that are compatible with silicon technology such as Ti or Co, were fabricated on top of them [26]. Thermal annealing of the contacts, which in the case of Ti electrodes led to the formation of TiC, produced a stronger coupling between the metal and the nanotube and a reduction of the contact resistance [26], [27].

Fig. 4(a) and (b) shows the output and transfer characteristics of such a CNTFET with Co electrodes [26]. From the $I_d - V_{gs}$ curves we see that the transistor is p-type and has a high on–off current ratio of $\sim 10^6$. This new CNTFET configuration has a significantly reduced contact resistance, $\sim$ 30 kΩ, a much higher current in the μA range, and a transconductance $g_m = 0.34\ \mu$S, i.e., $\sim$200 times higher than that of van der Waals-bonded CNTFETs.

All of the early devices were back-gated with very thick gate insulators (SiO_2 thickness $t_{\mathrm{ox}} \approx$ 100-150 nm). As with conventional MOSFETs we should be able to improve their performance by increasing the gate capacitance by reducing the insulator thickness or increasing the dielectric constant. However, unlike in the MOSFET configuration where the capacitance is similar to that of a plane capacitor, i.e., gate capacitance $C_G \sim 1/t_{\mathrm{ox}}$, the CNTFET geometry will predict a $C_G \sim \ln^{-1}(at_{\mathrm{ox}} + b)$ dependence [25]. In addition to increasing the gate capacitance, it is essential that each CNTFET is gated independently by its own gate so that complex integrated circuits can be built.

A next generation of CNTFETs with top gates was fabricated by dispersing SWCNTs on an oxidized wafer. Atomic

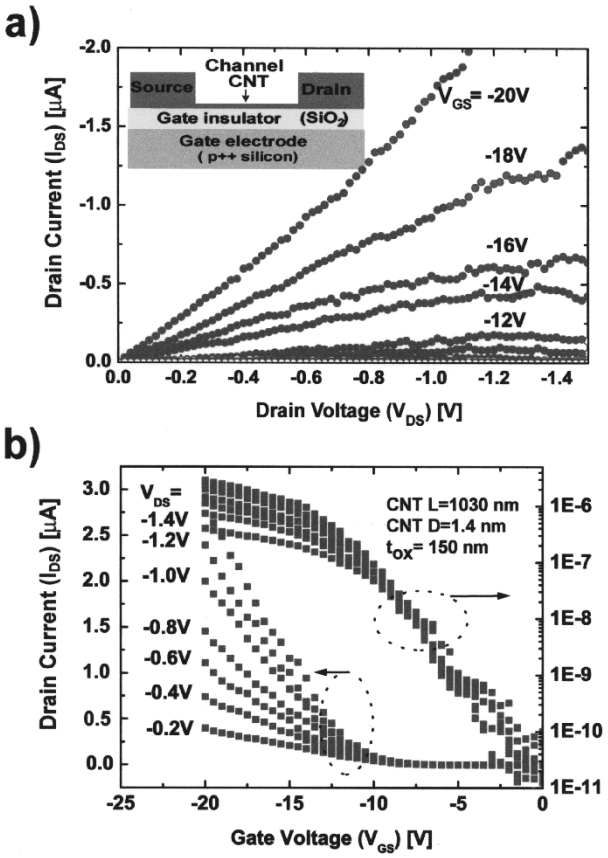

Fig. 4. (a) Output characteristics of a CNTFET with cobalt source and drain electrodes deposited on top of tube. (b) The corresponding transfer characteristics.

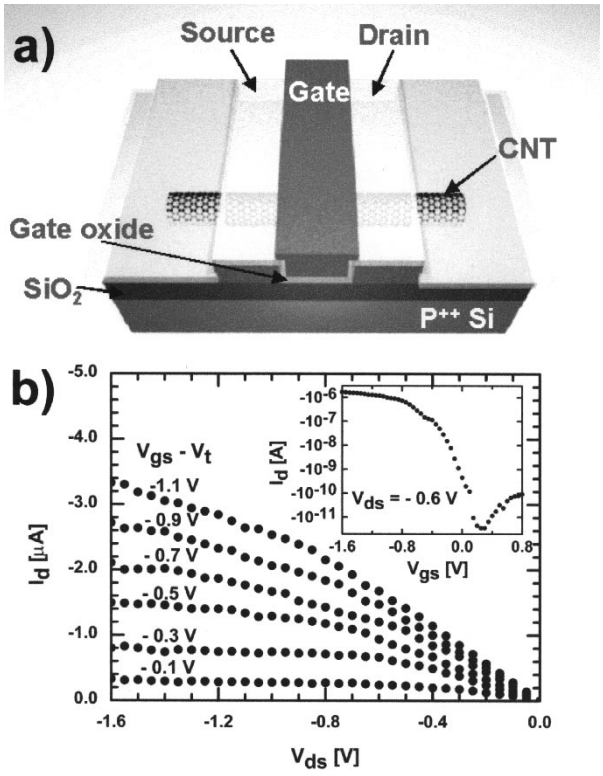

Fig. 5. (a) Schematic representation of one of our top-gated CNTFET with Ti source, drain, and gate electrodes. A 15-nm SiO_2 film was used as the gate oxide. (b) The *I–V* characteristics of the device.

force microscopy (AFM) imaging was used to identify single CNTs, and the Ti source and drain electrodes were fabricated on top of by e-beam lithography and liftoff [28]. After annealing at 850 °C to transform the contacts into TiC [27], a 15- to 20-nm-gate dielectric film was deposited by chemical vapor deposition (CVD) from a mixture of SiH_4 and O_2 at 300 °C. After annealing for ∼0.5 h at 600 °C in N_2 to densify the oxide, 50-nm-thick Ti or Al gate electrodes were patterned by lithography and liftoff.

In Fig. 5(a) we show a schematic of a top-gated CNTFET, and in Fig. 5(b) the output characteristics of such a device with Ti electrodes and a 15 nm SiO_2 gate insulator film [28]. Such a CNTFET can also be switched by the bottom gate (wafer) and the resulting characteristics can be compared with those of the device under top-gate operation. This device has a superior performance; the threshold voltage of the top-gated CNTFET is significantly lower, −0.5 V, than under bottom-gated operation, −12 V. Similarly, the drive current is much higher under top gating, and the transconductance is similarly high, $g_m = 3.3\ \mu$S per nanotube.

Since the eventual objective of nanotube electronics is to be competitive with silicon electronics, it is important to compare their relative performances, despite the fact that the CNTFETs are still far from being optimized. In these experiments a single SWCNT is used, so we express the current carrying capabilities of the devices per unit width (per micrometer) as is the practice in microelectronics. The

Table 1
Comparison of Key Performance Parameters for a 260 nm-Long Top Gate p-CNTFET, a 15-nm-Bulk Si p-MOSFET, and a 50-nm SOI p-MOSFET

	p-type CNTFET	Ref a	Ref. b
Gate Length (nm)	260	15	50
Gate oxide thickness (nm)	15	1.4	1.5
V_t (V)	-0.5	~-0.1	~-0.2
I_{ON} (μA/μm) ($V_{DS} = V_{GS} - V_t \sim -1$ V)	2,100	265	650
I_{OFF} (nA/μm)	-150	<-500	-9
Subthreshold slope (mV/dec)	130	~100	70
Transconductance (μS/μm)	2,321	975	650

a) B. Yu et al. IEDM Tech. Dig. 2001, p. 934; b) R. Chau et al. IEDM Tech. Dig. 2001, p. 621

diameter of the s-SWCNTs used was ∼1.4 nm. Table 1 shows the comparison of the characteristics of the CNTFET with two recent high-performance Si p-channel devices: a 15-nm-gate length MOSFET built on bulk silicon [29] and a 50-nm-gate length device built using SOI technology [30]. We also note that an optimal device layout may require the use of an array of CNTFETs. In this case the results can be scaled to give the total current for the array [26]. The current would increase the denser the packing of the tubes. However, screening at close separations can reduce the actual current per CNT by up to a factor of ∼2 [31].

From Table 1 we see that the CNTFET is capable of delivering three to four times higher drive currents than the Si MOSFETs at an overdrive of 1 V, and has about four times higher transconductance. From the above and other considerations, it is clear that CNTFETs, even in this early stage of de-

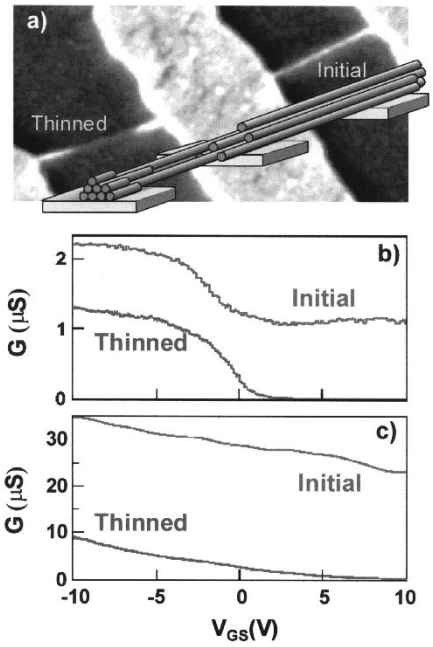

Fig. 6. Conductance (G) as a function of gate voltage ($V_{\rm GS}$) of a CNT bundle containing both metallic and semiconducting nanotubes before and after selective breakdown of the metallic CNTs. (a) Images of the intact and thinned nanotube bundle. (b) G versus $V_{\rm GS}$ for a thin bundle. (c) The same for a very thick bundle. In the latter case some semiconducting tubes had to be sacrificed in order to remove the innermost metallic tubes in the bundle.

velopment, can be very competitive with the corresponding Si devices. Further refinements can be expected by additional reductions in $t_{\rm ox}$ and the use of high-ε insulators. We have already seen significant improvements by using HfO_2 as a gate insulator [32], [52]. An insight to the ultimate potential of CNTFETs is provided by a recent study [33]. In this nanotube FET, the role of the gate was played by a droplet of an electrolyte connected to an electrochemical electrode. The combination of an electrolyte dielectric constant of about 80 and of the ultrathin ($\sim$0.5 nm) Hemholtz layer in the electrolyte led to an extremely high transconductance of about 20 μS. Further opportunities for improvements in the CNTFET performance arise from new insights on the switching mechanism in the CNTFET, as will be discussed in Section V.

IV. Transistors From Nanotube Bundles: Bundle Composition Engineering

A major impediment to the large-scale fabrication of CNTFETs is the fact that the current synthetic schemes for SWCNTs generate mixtures of metallic (m) and semiconducting (s) nanotubes. These tubes tend to adhere to each other, forming "bundles," or "ropes" [34]. No good methods exist for the preparation of only m- or s-CNTs by selective synthesis or postsynthesis separation. If CNTFETs were to be fabricated from such a bundle, the m-CNTs in the bundle would short out the device, as shown in Fig. 6. Currently, dilute suspensions of CNT bundles are ultrasonicated and dispersed on a wafer. AFM imaging is then used to identify isolated CNTs to build the CNTFET. We have developed

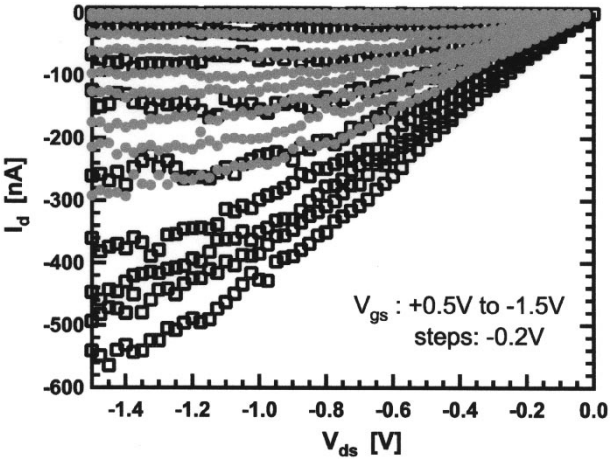

Fig. 7. Drain current versus gate voltage curves of a CNTFET upon interchange of its source and drain [32], [52].

the technique of "constructive destruction" [20] that allows us to selectively destroy the m-CNTs in a rope, leaving the s-CNTs intact.

As we discussed earlier, CNTs can carry enormous current densities at low electron energies. At higher energies, however, optical phonon excitation is possible [35], [36]. This leads to current saturation and the deposition of large amounts of energy, which eventually destroys the CNT structure [36]. To apply this method to remove m-CNTs from bundles, we first deposit the bundles on an oxidized Si wafer, then we fabricate on them an array of source drain and side gate electrodes. By applying an appropriate voltage bias to the gate, the s-CNTs can be depleted of their carriers. Then when a sufficiently high source-drain bias $V_{\rm ds}$ is applied, the generated current passes only through the m-CNTs, leading to their destruction, while leaving the s-CNTs essentially intact (see Fig. 6) [20]. In this way arrays of CNTFETs can be generated [20].

V. The Switching Mechanism of Carbon Nanotube Transistors

Up to this point we have implicitly assumed that the CNTFET switching mechanism is the same as that of conventional silicon devices. However, a number of observations suggest otherwise. For example, Fig. 7 shows the I_d versus $V_{\rm ds}$ curves for the same CNTFET upon interchange of the source and drain [32], [52]. A different current is obtained in the two cases. If the operation of the device were to be dictated by the properties of the bulk CNT, then the saturation current would be the same, since both sets of curves are taken with the same CNT. However, the different characteristics can be accounted for if transport in the tube is dominated by barriers (Schottky barriers[1]) at the CNT–metal contacts. In that case a small asymmetry of the barriers at the source and drain junctions could result in different saturation

[1]We use the term Schottky barriers in its most general sense to account for band bending in a semiconductor at a metal/semiconductor interface. When arguing about the switching in CNT transistors, we assume that there is no additional barrier present in our devices.

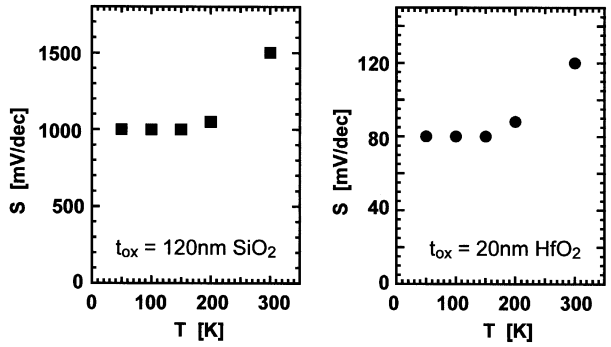

Fig. 8. Temperature dependence of the inverse subthreshold slopes, S, of two CNTFETs with 120 nm of SiO_2 and 20 nm of HfO_2 gate oxides, respectively [32], [52].

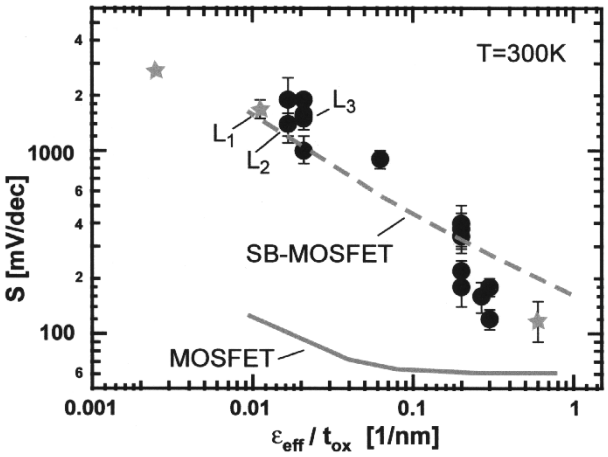

Fig. 9. Dependence of the inverse subthreshold slope S on the ratio $\varepsilon_{\rm eff}/t_{\rm ox}$, where $\varepsilon_{\rm eff}$ is the effective dielectric constant and $t_{\rm ox}$ is the thickness of the gate oxide. The points are experimental data from our own work, as well as from the literature. The solid line is the predicted behavior for bulk switching, while the dashed line is the prediction for the Schottky barrier switching model [32], [52].

currents. Further support for the existence of these barriers comes from the study of the subthreshold characteristics of CNTFETs.

In long-channel FET devices, the drain current I_D varies exponentially with V_G, and for drain bias $V_D > 3$ k_BT/q it is essentially independent of V_D [37]. A device characteristic of particular importance is the gate-voltage swing, or inverse subthreshold slope S. This is given by $S = \ln 10 \cdot {\rm dV}_G/d(\ln I_D) \simeq (k_B{\rm T/q}) \cdot \ln 10(1 + C_D/C_G)$. For a fully depleted device, the depletion capacitance C_D is zero; therefore, the second term in parenthesis becomes one. CNTs are a perfect example of a device exhibiting $C_D = 0$, since no charge variation can occur across the tube circumference. Under these ideal conditions S depends only on the temperature and has a value of 60 mV/dec at 300 K. Deviations appear when interface trap states are present in the oxide [37]. The capacitance due to these interface states $C_{\rm int}$ is in parallel with the depletion capacitance. The early back-gated CNTFETs with thick (100–150 nm) gate oxides had unexpectantly high S values of 1–2 V/dec. Devices with thin oxides, such as the top-gated CNTFET in Fig. 5, have S$\sim$100–150 mV/dec. Interface traps could in principle account for these observations. However, we found that the high S values for thick oxides are very similar independent of whether an n-type, a p-type, or an ambipolar transistor was measured. Since there is no doubt about the presence of Schottky barriers in case of an ambipolar device, and—as we proved [32], [52]—a Schottky barrier model alone can explain the trend of S as a function of $t_{\rm ox}$ quantitatively, interface traps are not responsible for the high S values in case of thick gate oxides. Further evidence that S is determined by Schottky barriers comes from its temperature dependence. As can be seen from Fig. 8, S is temperature dependent at higher temperatures but levels off at temperatures below about 200 K, suggesting a carrier tunneling process. The described subthreshold behavior may be unexpected for a bulk-switched device, but can be fully accounted for by a Schottky barrier transistor model [32], [52]. Calculations of S as a function of $t_{\rm ox}$ based on the SB and bulk models along with our own and literature experimental data are shown in Fig. 9. The data are fitted well by the SB model but not by the bulk switching model.

Focusing on the Schottky barrier itself, we note that the electrostatics in 1-D is different than that in 3-D and it is reflected in the shape of the barriers [38]. In 1-D the barriers are thin, showing an initial sharp drop followed by a logarithmically decreasing tail. Because of the thinness of the barrier, tunneling in 1-D is easy and can dominate transport. In Fig. 10(a) we show the schematic of a top-gated CNTFET and the electric field generated by the gate in that structure. Fig. 10(b) gives the conductance of the device as a function of the gate voltage for different values of the Schottky barrier height. Finally, Fig. 10(c) shows the source Schottky barrier for a mid-gap CNT at three different gate voltages [38]. The shape of the barrier and the thinning resulting from the gate field can be clearly seen.

The SB model can also provide an explanation for the long-standing problem involving the effect of the ambient on the performance of CNTFETs. Already in the first studies of CNTFETs, it was observed that although the CNTs used were not intentionally doped, the fabricated CNTFETs were p-type [24], [25]. These early FETs were fabricated in air. It was later found that when CNTs are placed in vacuum, their electrical resistance increased and their thermopower changed sign [40]. It was proposed that the CNTs transfer electrons to atmospheric O_2 and, thus, become doped with holes [41].

We have performed detailed studies of this gas effect on nanotubes in a CNTFET configuration [42]. In our early studies, we used a back-gated FET configuration with a thick (100–150 nm) gate oxide. As Fig. 11 shows, initially the air-exposed CNTFET was p-type. However, after annealing under vacuum becomes n-type. Furthermore, as Fig. 11 shows this unexpected transformation is reversible; reexposure to O_2 brings back the p character of the FET. Intermediate stages where the CNTFET exemplifies *ambipolar* behavior are clearly seen.

The above findings prove that the p character of the CNTFET is not an intrinsic property of the CNTs, but results

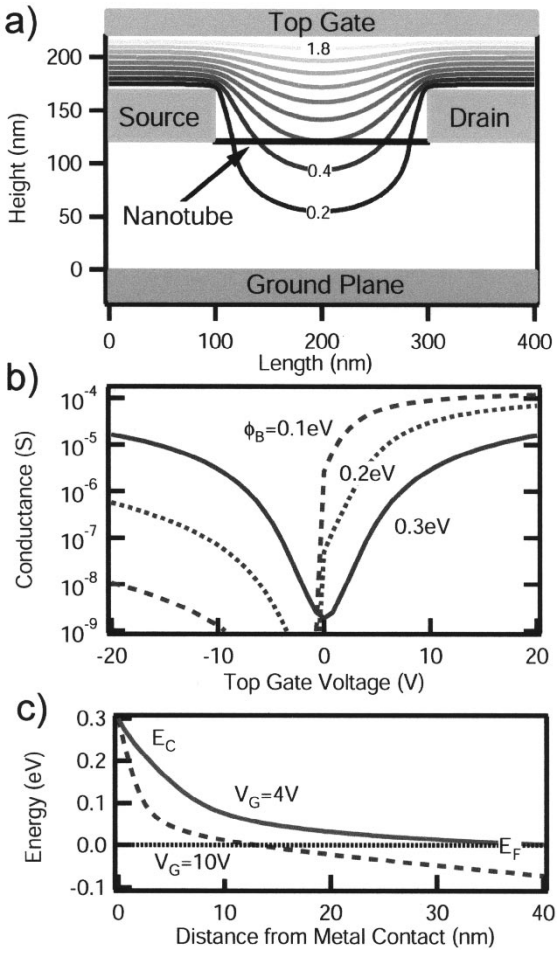

Fig. 10. Simulation of the operation of a top-gated Schottky barrier CNTFET. (a) The structure of the CNTFET and the electric field lines ($V_{\rm gate} = 2$ V). (b) Conductance versus gate voltage for different values of the Schottky barrier. (c) The effect of gate bias on the Schottky barrier at the source–CNT junction [39].

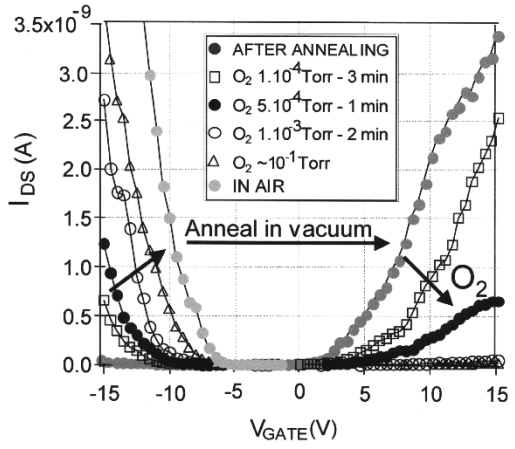

Fig. 11. Transformation of a p-type CNTFET by annealing in vacuum into an n-type CNTFET and the reverse transformation upon exposure to O_2. The transformation proceeds via ambipolar intermediate states of the CNTFET. No threshold shifts are observed, and the drain current at $V_{\rm GATE} = 0$ does not change.

from the interaction with O_2. We have performed a number of experiments to ascertain the nature of this interaction. In Fig. 12 we show the behavior of a CNTFET upon doping

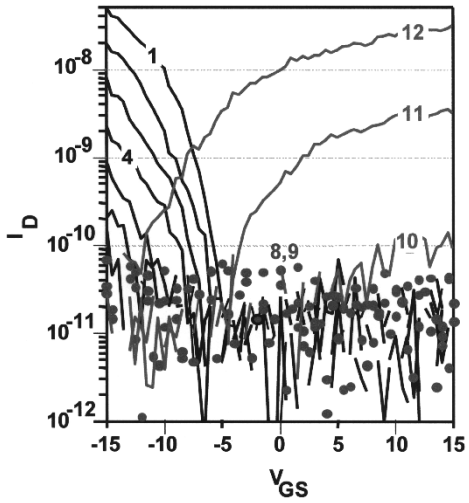

Fig. 12. The effect of doping with increasing amounts of potassium on the electrical characteristics of an initially p-type (curve 1) CNTFET.

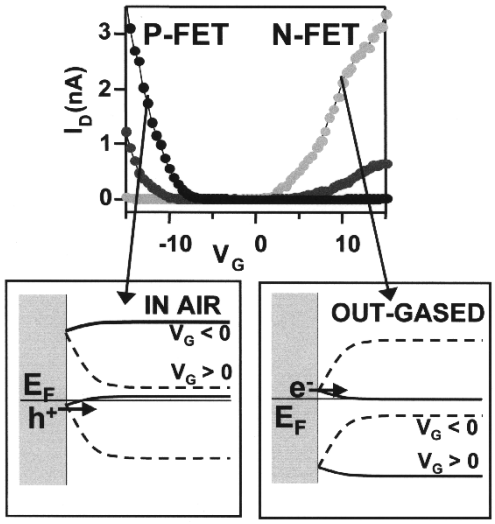

Fig. 13. Qualitative diagram showing the lineup of the valence and conduction bands of a CNT with the metal Fermi level at the source–CNT junction first in air and after annealing in vacuum.

with an electron donor, in this case potassium [42]. The well-known characteristics of doping, i.e., a shift of the threshold gate voltage and an increasing current at $V_g = 0$, are clearly seen. However, this behavior is in stark contrast with the behavior observed upon O_2 exposure (see Fig. 11). From this and other experiments, we have concluded that although some doping by O_2 may take place, this by itself cannot account for the observed behavior.

As we have already shown above, transport and switching in CNTFETs is controlled by the Schottky barriers at the contacts. Oxygen then must affect these barriers. When a nanotube is bonded to a metal electrode the resulting charge transfer determines the lineup of the nanotube bands. However, this charge transfer and the resulting field can be strongly affected by the coadsorption of other species such as oxygen near or at the CNT–metal junction. These coadsorbates can change locally the surface potential [39] or

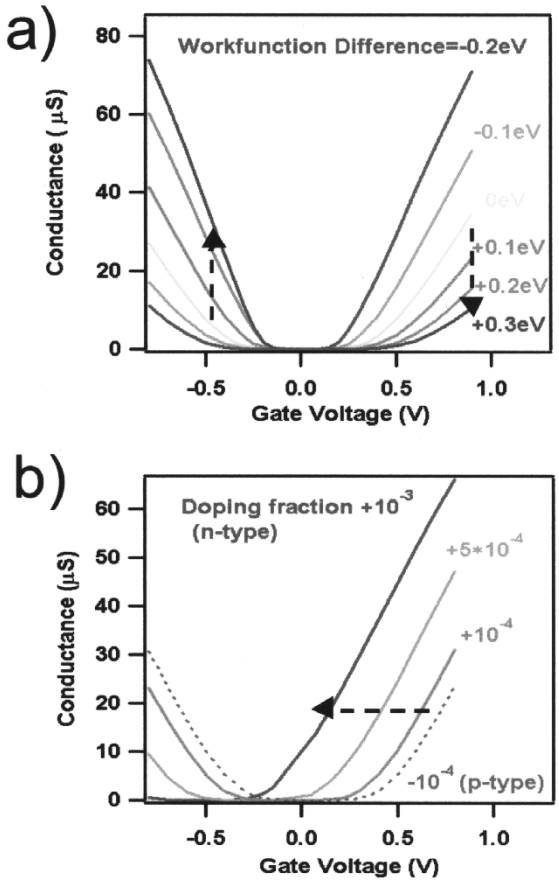

Fig. 14. Simulations of the effect of O_2 and K on the CNTFETs current–voltage characteristics [39].

directly interact with the junction [43]. In Fig. 13 we give a schematic that accounts qualitatively for the band lineup at a metal–CNT junction in air and after annealing in a vacuum. The p character in air is the result of Fermi level pinning near the valence band maximum.

Support for this interpretation is provided by theoretical modeling. In order to take advantage of the simpler electrostatics, we used a model of a CNT surrounded by a cylindrical gate. In Fig. 14 we simulate the I–V characteristics of a CNTFET upon oxygen adsorption by changing the local surface potential [39]. Although the numbers cannot be compared because of the different device geometry used in the calculation, it is clear that the resulting behavior is similar to that of Fig. 11. In contrast, a model where fixed charges are placed along the length of the tube in order to simulate a doping interaction gives a behavior similar to that of doping by potassium in Fig. 12.

The effect of oxygen dominates the behavior of CNTFETs as long as the gate field is weak. This was the case for our earlier structures with thick gate oxides. However, in our recent CNTFETs with thin oxides ($t_{\rm ox}$ ~2–5 nm), we observe ambipolar characteristics even in air, indicating a near midgap lineup of the CNT bands [53]

VI. Multiwalled Nanotube Field-Effect Transistors

Our discussion above has been limited to transistors made out of SWCNTs. Low-temperature studies of the

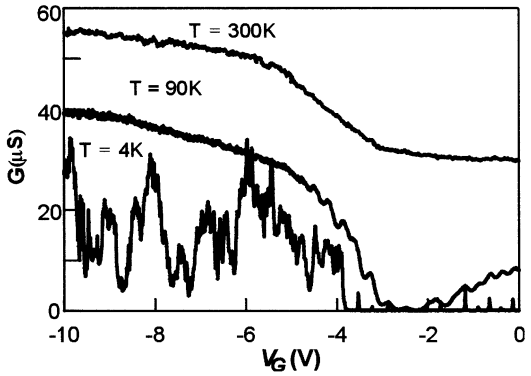

Fig. 15. Temperature dependence of the conductance G of an MWCNT as a function of the gate voltage.

Aharonov–Bohm effect in MWCNTs have concluded that in MWCNTs side-bonded to metal electrodes, effectively only the outer shell contributes to electrical transport [22]. One would expect then that MWCNTs with a semiconducting outer shell could be used to fabricate CNTFETs. However, in semiconducting CNTs, the band gap ($E_{\rm Gap}$) is inversely proportional to the tube diameter; therefore, only small-diameter MWCNTs are expected to display large switching ratios at room temperature.

In Fig. 15 we show the effect of the gate voltage V_G on the conductance G of a 14-nm diameter MWCNT, at different temperatures [21]. Clearly, the gate can modulate the conductance of the MWCNT channel at room temperature. However, there is a large residual conductance, which can be assigned to the coupling of the outer semiconducting shell to an inner metallic shell. This coupling is expected to be activated with an activation energy of the order of $\sim E_{\rm Gap}/2$. At low temperatures, the contribution of the inner metallic shell is suppressed (see Fig. 15). These observations indicate that the transport characteristics of an MWCNT at ambient temperature may have contributions from more than the outer shell even for side-bonded CNTs. Because of the activated nature of the shell-to-shell transport, and given that the semiconducting gap is inversely proportional to the CNT diameter, multishell transport should be more important for large-diameter tubes.

When the applied $V_{\rm DS}$ is increased, the average energy of the carriers is expected to increase, as well as the coupling between the carbon shells. As we discussed in Section IV, higher electron energies lead to energy dissipation and breakdown. Our studies of MWCNTs have shown that initiation of the breakdown occurs at a power threshold, which is significantly lower in air than in vacuum [36]. This indicates that an "oxidation" process takes place in air. The oxidation is most likely not a purely thermal process. Calculations on graphite have shown that once certain defects are generated, e.g., di-vacancies, a self-sustaining chain reaction with oxygen can take place [44]. Because of the lower breakdown threshold in air, the shell breakdown in MWCNT proceeds sequentially from the outer to the inner shells. This shell-by-shell breakdown can be seen as a stepwise decrease in the current flowing through the CNT [see Fig. 16(a)]. It is also illustrated by AFM images of an MWCNT draped over

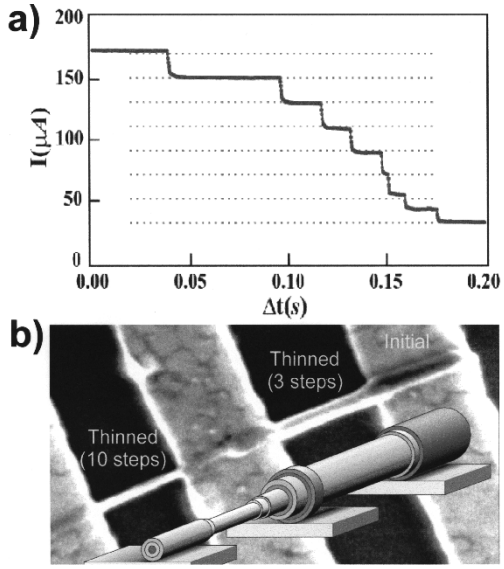

Fig. 16. (a) Stepwise decrease of the current during the breakdown of an MWCNT. (b) Images of an MWCNT showing part of the initial tube, as well as segments of the same MWCNT from which three and ten carbon atom shells have been removed.

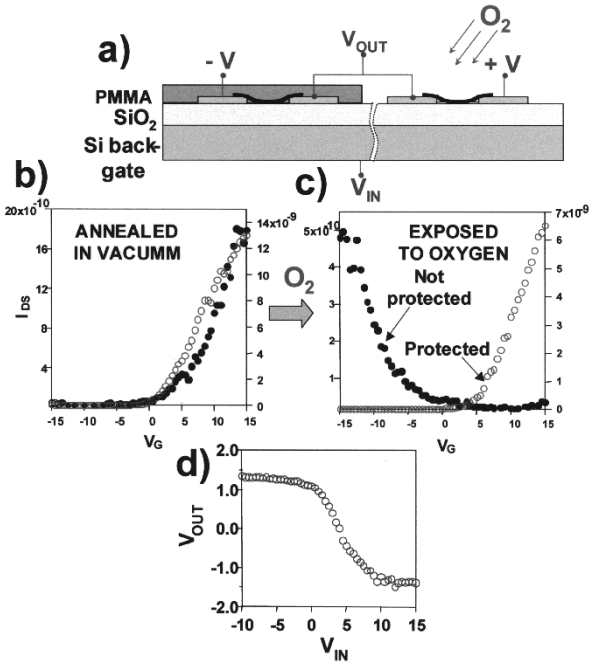

Fig. 17. (a) Schematic representation of the internanotube voltage inverter (NOT gate). One of the FETs is protected by a layer of PMMA. (b) After annealing two p-CNTFETs in vacuum to form two n-type CNTFETs. (c) After exposure to oxygen at 300 K. (d) Electrical behavior of the inverter.

several metal electrodes, so that individual CNT segments can be electrically stressed independently. Thinned segments that have lost three and ten shells, respectively, as well as a portion of the initial MWCNT, are clearly seen [Fig. 16(b)]. The capability to remove carbon atom shells one by one and identify their character through the effect of the gate field [20], [21], along with the diameter dependence of the band gap ($E_{\mathrm{Gap}} \sim 1/d_{\mathrm{CNT}}$) allows the fabrication of CNTFETs with a desired E_{Gap} can be fabricated using the controlled breakdown process.

VII. Carbon Nanotube Integrated Circuits: Logic Gates

So far we have concentrated our discussion on the performance of individual CNTFETs. The fabrication of integrated circuits using such devices is the next step. In 2001 we demonstrated that this was possible by fabricating a CMOS-like voltage inverter (a logic NOT gate) [45]. For simplicity, we used the early design of CNTFETs involving the CNT on top of gold electrodes

In Fig. 17 we show the structure and electrical characteristics of an inverter circuit involving a n- and a p-CNTFETs. Originally, both CNTFETs were p-type because of their exposure to air (oxygen). We then covered one of them by a protective film of PMMA (a more stable protection is provided by a SiO_2 film [27]), while the other was left unprotected. Both of the CNTFETs were then annealed under vacuum, which transformed both of them into n-type. After cooling, the pair was exposed to oxygen, which converted the unprotected CNTFET to p-type, while the protected one remained n-type. In this way, the two complementary CNTFETs needed were formed and wired.

The inverter works the same way as an ordinary CMOS inverter. The input voltage is applied simultaneously to the gates of the complementary CNFETs. The p-CNFET is polarized by a positive voltage, the n-FET by a negative voltage, and a common contact is used as the intermolecular inverter's output. A positive input voltage turns the n-CNFET "on" (the p-CNFET being "off"), resulting in the transmission of the negative voltage to the output. A negative input, on the other hand, turns the p-CNFET "on," producing a positive output. The electrical characteristics of the CNTFETs at each stage and those of the resulting inverter are shown in Fig. 17. We refer to this inverter circuit as an *intermolecular* inverter because it involves two nanotube molecules.

Ideally, one would like to achieve the ultimate level of integration by fabricating the circuits along the length of a single CNT, i.e., form an *intramolecular* circuit. A first realization of this approach is shown in Fig. 18(a) [44]. As the AFM image shows, the nanotube is placed on top of three prefabricated gold electrodes. In this way two back-gated initially p-type CNTFETs are formed. Then they are both covered by PMMA and a window is opened by e-beam lithography over the channel of one of them. Through this window, the channel is n-doped using potassium as a dopant. In this way two complementary FETs are formed along the same nanotube. The electrical characteristics of the resulting inverter are shown in Fig. 18(b). It is particularly interesting that despite the fact that no effort was made to optimize the construction and performance of the individual CNTFETs, the resulting inverter had a gain of almost two. This suggests that optimized CNTFETs would lead to much higher gain and can be wired along the length of a single CNT to produce more complex circuits. Following this initial work [45], more nanotube logic gates of complementary [46] or transistor–resistor [47] type have been demonstrated.

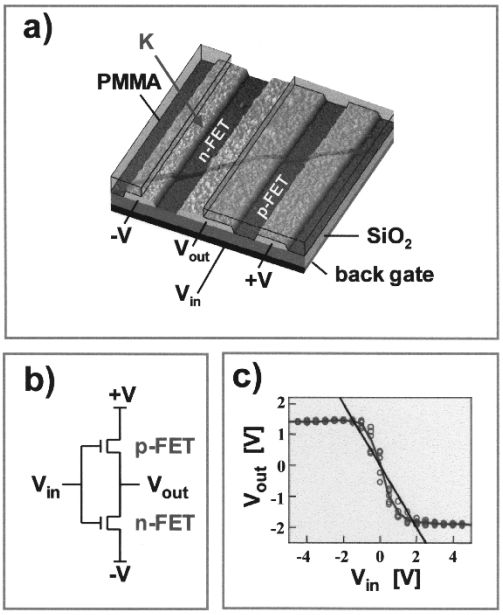

Fig. 18. (a) Atomic force microscope image of the intrananotube voltage inverter. (b) Schematic of the inverter. (c) Electrical behavior of the intrananotube inverter.

VIII. Nanotube Synthesis

SWCNTs are produced using arc discharges [2], [3], laser ablation of a carbon target [34], or CVD [48]. In all of these techniques, a metal catalyst (typically Co, Fe, and/or Ni) in the form of nanoparticles is utilized.

Currently, catalytic CVD is the most widely used technique [48]. One of the advantages of this approach is that it allows nanotubes to be grown locally by placing the catalyst at the appropriate location [49]. We have experimented with catalytic CVD using a combination of electrolytic and lithographic approaches to control both the location and orientation of the growth. The procedure shown in Fig. 19 involves the following steps:

1) patterning a thin, heavily doped silicon surface layer lithographically;
2) electrolytically etching the silicon to form porous silicon on the sidewalls of the patterned structure;
3) protecting with photoresist the areas of the silicon surface where we do not want CNT growth;
4) driving into the exposed pores the metal catalyst, and after removing the rest of the photoresist, reacting with CH_4 at $\sim$ 1000 °C to form SWCNTs.

Fig. 20 shows SEM images of SWCNTs grown this way bridging adjacent silicon pads. These pads can subsequently be metallized.

Quite often, the presence of heavy metal catalyst particles in the nanotube product is unwanted but their removal is problematic and usually leads to damaged nanotubes. In applications in nanoelectronics, it is also likely that arrays of parallel oriented tubes will be needed in order to reduce the impedance of the devices and provide a high drive current [26]. Oriented growth of tubes is a very desirable way to achieve this type of nanotube organization. Postsynthesis alignment has also been pursued [50].

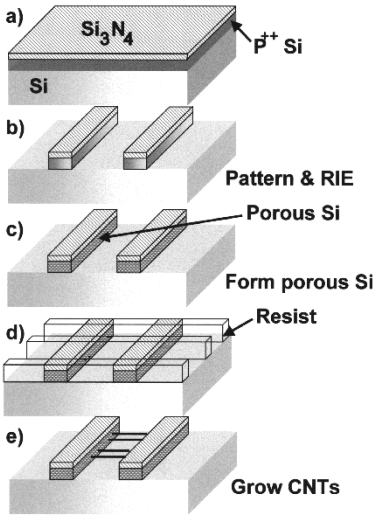

Fig. 19. Sequence of lithographic and other processing steps used to produce selective local growth of SWCNTs by chemical vapor deposition using CH_4 as the source of carbon.

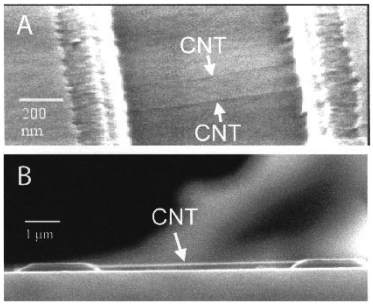

Fig. 20. Electron microscope images (top and side views) showing locally grown CNTs connecting silicon electrodes.

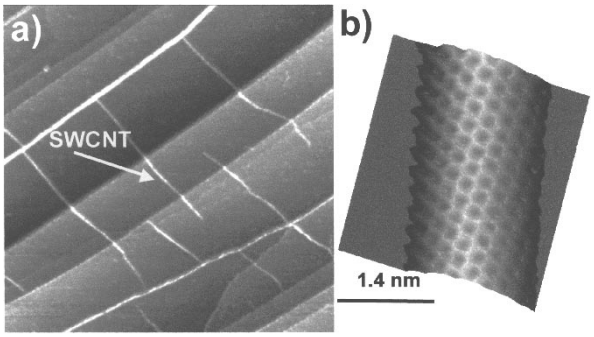

Fig. 21. (a) STM image of oriented (parallel) SWCNTs produced by heating under high vacuum to 1650 °C a 6 H-SiC wafer with a (0001) Si-face. (b) Atomic resolution STM image of a SWCNT produced by this method.

Recently, we discovered a way to produce oriented SWCNTs by a catalyst-free approach [51]. This approach involves the thermal annealing under vacuum of SiC crystals. Specifically, 6H–SiC wafers with a polished (0001) Si face (this surface is equivalent to the (111) surface of cubic SiC (3 C–SiC)) were heated to 1650 °C at $P < 10^{-9}$ torr.

Fig. 21(a) shows a scanning tunneling microscope (STM) image of a sample cut along the (1,−1,0,0) axis of the wafer resulting in a morphology characterized by well-ordered

parallel steps in the (1,1,−2,0) direction. The white 1-D structures, identified as the CNTs, extend over several steps or terraces and are not present on the samples annealed in vacuum at a temperature below 1400 °C. An atomic resolution image of a semiconducting nanotube is shown in Fig. 21(b). From such images, as well as TEM images, the diameter of the nanotubes produced was determined to be in the range of 1.2–1.6 nm. These tubes are seen to have their axis perpendicular to the surface steps or be aligned along the steps. Extensive STM and AFM studies showed that this organization is uniform over their entire area of the sample. When the surface morphology is composed of terraces, the nanotubes form a weblike network with a predominance of 120° angles between straight sections (not shown) [51].

Along with individual SWCNTs, thicker tubes are also observed. Manipulation experiments using the tip of an AFM [51] indicate that these structures are SWCNT bundles, not MWCNTs.

The orientation of the nanotubes could be a result of the growth process or may involve a postsynthesis rearrangement. Our AFM experiments show that the tubes are mobile on the surface at the high temperature used for their formation. This is deduced by the observation that after perturbing the structure of the nanotubes by AFM manipulation, annealing at a temperature of 1300 °C, i.e., at a temperature lower than that needed for nanotube formation, brings the manipulated nanotubes back to their parallel orientation. Thus, we believe that the orientation of the nanotubes results from their motion that releases part of the mechanical stress incorporated in the randomly grown network by favoring straight segments and by matching their orientation to the crystallographic structure of the surface. At the same time, formation of bundles contributes to the lowering of the total energy.

The above findings suggest that: 1) it may be possible to orient preformed nanotubes on an inert substrate by heating them at a temperature at which they acquire sufficient mobility and 2) in principle, it is possible to synthesize nanotubes in a controlled manner by patterning graphene strips followed by annealing. By selecting the direction of the cut of the strip, the chirality of the resulting nanotube can be chosen.

IX. Conclusion and the Future

CNTs are new materials with outstanding electrical properties. The high conductivity and exceptional stability of metallic nanotubes makes them excellent candidates for future use as interconnects in nanodevices and circuits. FETs using semiconducting CNTs have operating characteristics that are as good as or better than state-of-the-art silicon devices, and significant improvements should be expected in the near future. However, while CNTs are one of the most promising materials for molecular electronics, many challenges remain before they can become a successful technology. Most challenging are the materials issues. We still lack a method that produces a single type of CNT. In this respect, seeded growth techniques are a possibility and need to be explored. Another possible solution involves the development of efficient separation techniques, and work is pursued in this direction with encouraging initial results. The sensitivity of the electrical properties of CNTs and CNT devices to the nature of the CNT–metal contacts and the ambient environment demonstrated in this article shows that better understanding and control of these problems is absolutely essential. For CNT device integration, new fabrication techniques that are based on self-assembly of CNTs are highly desirable. While our own current interest is in computer electronics, it is likely that the initial applications of CNT devices will be in less integrated systems such as sensors, or in special applications where devices of exceptional miniaturization and performance are needed. Apart from their technological importance, CNTs are ideal model systems for the study and understanding of transport in 1-D systems and for the development of molecular fabrication technologies.

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Phaedon Avouris (Member, IEEE) received the B.S. degree from Aristotelian University, Thessaloniki, Greece, in 1968 and the Ph.D. degree in physical chemistry from Michigan State University, East Lansing, in 1974.

After postdoctoral work at UCLA and AT&T Bell Laboratories, he joined the Research Division of IBM in 1978. He is currently Manager of Nanometer Scale Science and Technology at the IBM T. J. Watson Research Center, Yorktown Heights, NY, and Adjunct Professor at Columbia University, New York, and the University of Illinois, Urbana-Champaign. He has published about 300 scientific papers. He is currently serving on the Advisory Editorial Board of *Nano Letters*, *Nanotechnology*, *Surface Review and Letters*, and the *Journal of Electron Spectroscopy*. He is also Coeditor of the Springer-Verlag (Berlin, Germany) book series on nanoscience. Over the years, his research has involved a wide variety of subjects ranging from laser studies of fast phenomena, surface physics and chemistry, scanning tunneling microscopy and atom manipulation. His current research is focused on experimental and theoretical studies of the electrical properties and transport mechanisms of carbon nanotubes, molecules and other nanostructures.

Dr. Avouris has been elected Fellow of the American Academy of Arts and Sciences, the American Physical Society, the American Vacuum Society, the American Association for the Advancement of Science and the New York Academy of Sciences. He is also a Member of the American Chemical Society and the Materials Research Society. He received the Irving Langmuir Prize of the American Physical Society, the Medard W. Welch Award of the American Vacuum Society, the Feynman Prize from the Foresight Institute, the ACSIN Nanoscience Prize, the Distinguished Alumnus Award from Michigan State University, and several IBM Corporation "Outstanding Technical Achievement" awards.

Joerg Appenzeller received the M.S. and Ph.D. degrees in physics from the Technical University of Aachen, Aachen, Germany, in 1991 and 1995. respectively. His Ph.D. dissertation investigated quantum transport phenomena in low-dimensional systems based on III/V heterostructures.

In 1995, he was a Research Scientist in the Research Center, Juelich, Germany. From 1996 to 1998, he was an Assistant Professor with the Technical University of Aachen. During his professorship, he explored mesoscopic electron transport in different materials including carbon nanotubes and superconductor–semiconductor hybrid devices. From 1998 to 1999, he was a Visiting Scientist with the Massachusetts Institute of Technology, Cambridge, exploring the ultimate scaling limits of silicon MOSFET devices. Since 2001, he has been a Research Staff Member with the IBM T. J. Watson Research Center, Yorktown Heights, NY, mainly involved in the investigation of the potential of carbon nanotubes for a future nanoelectronics.

Richard Martel received the Ph.D. degree in physical chemistry from Laval University, Quebec, QC, Canada in 1995.

From 1995 to 1998, he did postdoctoral work at IBM. He is currently a Research Staff Member in the Nanometer Scale Science and Technology Group, T. J. Watson Research Center, Yorktown Heights, NY. His early work focused on electron excitations and dissociative electron attachment in molecules adsorbed on surfaces. His interest is now focused on the electrical properties of carbon nanotubes and electroactive molecular nanostructures.

Shalom J. Wind (Senior Member, IEEE) received the B.A. degree in physics from Yeshiva University, New York, in 1977 and the M.Phil. and Ph.D. degrees in physics from Yale University, New Haven, CT, in 1987, where he studied electron quantum transport in metallic nanostructures.

From 1987 to 2003, he was with the IBM T. J. Watson Research Center, Yorktown Heights, NY, where he focused primarily on the fabrication and study of nanostructures and nanodevices, including the first demonstration of a single electron transistor in a semiconductor system, fabrication of ultracompact silicon FETs, study of silicon devices near the limits of scaling, control of self-assembly of semiconductor quantum dots, as well as other novel electronic and magnetic nanostructures. He is currently a Senior Research Scientist in the Department of Applied Physics and Applied Mathematics, Columbia University, New York. He has also been active in the field of nanolithography, both in the application of lithography technologies to device fabrication, as well as in the development of innovative techniques in electron beam proximity effect correction. His current research focuses on molecular electronics, including the fabrication and characterization of carbon nanotube FETs, the controlled growth of carbon nanotubes for nanoelectronic applications, and the study of transport in single-molecule transistors.

Dr. Wind is a Member of the American Physical Society and the American Association for the Advancement of Science.