1 Carbon Nanotube Electronics and Optoelectronics

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Summary. In this chapter, we review progress to date in carbon nanotube electronics and optoelectronics. We discuss the underlying physics of CNT-FETs, highlighting the similarities and differences relative to conventional silicon metal-oxide-semiconductor field-effect transistors (MOSFETs), and we examine how these affect CNT-FET electrical characteristics. As device scaling is the key technology driver in today's semiconductor technology, we explore how CNT-FETs behave when scaled to smaller dimensions and the impact this scaling behavior may have on their suitability for technological insertion. We look at results achieved to date on simple CNT-based circuits, and we consider the requirements of more complex architectures. Finally, we discuss the optoelectronic properties of CNTs and show that CNT-FETs can also be used as light emitting and light decoding devices.

1.1 Introduction

The discovery of the integrated circuit by Jack Kilby at Texas Instruments has lead to four decades of dizzying advances in silicon-based electronic technology. This progress has been achieved primarily through the sustained scaling of physical dimensions in the metal-oxide-semiconductor field-effect transistor (MOSFET), which has lead to many successive generations of devices with increased transistor performance and density. Most experts agree that by continuing on this scaling path, the community will reach technological, economic and, most importantly, fundamental physical limits as soon as the end of this decade. Therefore it becomes crucial to start preparing for technologies that will enable continued implementation of increasingly higher performance devices.

In general, two distinct approaches are taken to address these issues. In one case, revolutionary technologies are proposed based on totally new concepts, for example two terminal molecular devices, spintronics, or quantum

computing may be pursued. While some of these technologies may one day be implemented into products, they are obviously targeted for the far future. We focus on another, more evolutionary approach that is based on the well established three terminal transistor concept, but utilizes different materials, specifically carbon nanotubes (CNTs) that may address many of the problems present in aggressively scaled silicon devices. Indeed, the silicon electronics industry has long experimented with progressively more radical alternative materials (such as SOI, SiGe and high-k dielectrics to name a few) in order to improve device performance. In this vein, single-walled CNTs (SWCNTs) have some unique advantages including their nanoscale dimensions as well as the electronic and optical properties which we will describe in this chapter. Specifically, we will describe the progress on carbon nanotube field-effect transistors (CNT-FETs) used in electronics as switches and opto-electronics as light-emitters/detectors. While current state-of-the-art devices contain individual CNTs, the results are applicable to CNT arrays for larger current or light signals, provided that synthesis of homogenous CNT samples is developed.

1.2 Electronic Structure and Electrical Properties of Carbon Nanotubes

A single-walled carbon nanotube can be thought of as a graphene sheet (i.e., a single layer of graphite) rolled up into a cylinder, as in Fig. 1a. Consequently, the electronic properties of single-walled carbon nanotubes can be derived directly from those of graphene [1–3], with unique characteristics resulting from the precise arrangement of the carbon atoms of the rolled up graphene sheet. This "rolling up" can be described in terms of the "chiral vector," $\mathbf{C}$ (see Fig. 1.1a),which connects two sites of the two-dimensional graphene sheet which are crystallographically equivalent: $\mathbf{C} = n\hat{\mathbf{a}}_1 + m\hat{\mathbf{a}}_2$, where $\hat{\mathbf{a}}_1$ and $\hat{\mathbf{a}}_2$ are the unit vectors of the hexagonal graphene lattice. The unit cell of the nanotube is defined as the rectangle formed by $\mathbf{C}$ and the one-dimensional translational vector,$\mathbf{T}$, as shown in Fig. 1.1a. Thus, the geometry of any nanotube can be described by the integer pair (n, m) which determine the chiral vector.

The band structure of graphene is quite unusual. It has states crossing the Fermi level at six points in k-space, as shown in Fig. 1.1b. The folding of the graphene layer to form a CNT introduces an additional level of quantization due to the confinement of electrons around the circumference of the nanotube. The component of the wave-vector $\mathbf{k}_c$ is constrained by the condition $\mathbf{k}_c \cdot \mathbf{C} = 2\pi j$, where j is an integer. Thus, in going from a 2D graphene sheet to a 1D CNT, each graphene band is split into a number of 1D subbands indexed by j, with allowed energy states corresponding to slices through the graphene band structure. Slices which pass through a K-point of the graphene Brillouin zone result in a metallic nanotube; all other slices yield semiconducting CNTs.

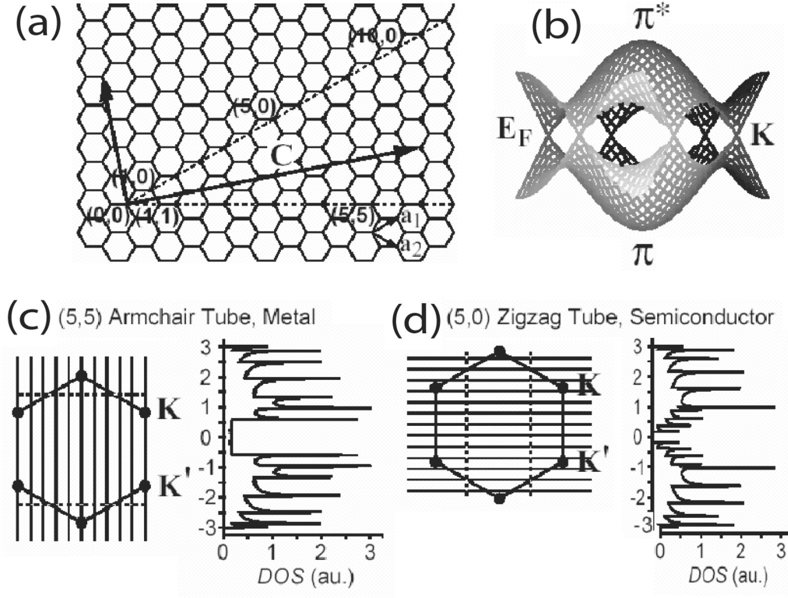

Fig. 1.1. (a) Definition of the chiral and translation vectors and the (n,m) notation of carbon nanotubes. **(b)** Band structure of the graphene layer. **(c)** and **(d)** Allowed 1D states as cuts of the graphene Brillouin zone for a (5,5) metallic (c) and a (5,0) semiconducting (d) nanotube, along with their associated density of states

Figs. 1.1c and 1.1d illustrate the contrasting cases of a metallic $(5,5)$ tube and a semiconducting $(5,0)$ tube, with their respective band structure and density of states in a π tight-binding description.

The general rules for determining whether a CNT is metallic or semiconducting based on the chiral indices (n,m) are: when $n = m$, the tube is metallic; when $n - m = 3i$, where i is a nonzero integer, the tube is a small-gap semiconductor; and all other combinations of (n,m) are true semiconductors. The band gap of semiconducting CNTs depends on the tube diameter. According to the tight-binding description of the electronic structure, the band gap, E_{gap} is given by $\gamma(2a/\sqrt{3}d_{CNT})$, where γ is the hopping matrix element, $a = \sqrt{3}d_{C-C}$, with d_{C-C} being the carbon-carbon bond distance, and d_{CNT} is the nanotube diameter [1–3].

The two-terminal conductance of a metallic single-walled CNT is given by the Landauer-Buttiker formula for one-dimensional conductors [4]: $G = (2e^2/h) \cdot \sum_i^N T_i$, where $2e^2/h$ is the quantum unit of conductance, and T_i is the transmission of the ith conducting channel. When $T_i = 1$, corresponding to the case of no scattering inside the nanotube or at the contacts, a metallic nanotube has a resistance, $R = 1/G = h/(4e^2)$, because there are 2 contributing conductance channels near the Fermi energy [5].

In the case of scattering within the CNT, an effective scattering length, λ_{eff}, can be used to describe the scattering. Multiple processes may contribute to scattering, and thus, $\lambda_{eff}^{-1} = \lambda_{el}^{-1} + \lambda_{ac}^{-1} + \lambda_{op}^{-1}$, where λ_{el} is the mean free path for elastic scattering, and λ_{ac} and λ_{op} are the mean free paths for scattering by acoustic and optical phonons, respectively. Due to the one-dimensional confinement of electrons on the surface of the nanotube, which allows only forward and backward motion, and the requirements for energy and momentum conservation, the available phase space for scattering is drastically constrained. The result is weak elastic scattering, with $\lambda_{el} \geq 1\mu m$, in the bulk of pure metallic CNTs. Acoustic phonons contribute weakly to inelastic scattering as well, with $\lambda_{ac} \approx 1\mu m$ [6]. Thus, transport in metallic CNTs at low excitations is ballistic over distances of a micron or so. Optical phonons can scatter efficiently at high excitations once carriers exceed optical phonon energies ($\sim 180meV$), with $\lambda_{op} \approx 20 - 30nm$ [7–9]. This can result in current saturation at elevated bias [7] and can lead to nanotube breakdown [11]. Thus far, there is somewhat less information on scattering in semiconducting CNTs, however, there are indications that at low excitations, λ_{eff} is of order a few hundred nanometers [10, 12, 13].

For the case of a CNT device in which a semiconducting nanotube is connected to metallic leads, there are other sources of contact resistance in addition to the Landauer resistance mentioned above: Schottky barriers form at the metal/nanotube junctions, through which carriers must tunnel [14]. These Schottky barriers have a profound effect on the function and performance of CNT-based transistors, as will be discussed below. Additional sources of series resistance, which are not intrinsic to the device itself, can in some instances make an overwhelming contribution to the total measured CNT resistance, as well.

1.3 Potential and Realized Advantages of Carbon Nanotubes in Electronics Applications

Having discussed the structure and properties of CNTs in Section 2 it is useful to understand the general material-based benefits that may translate in additional performance enhancements for CNT devices. Some of these attributes have already been demonstrated in experiments, while others have yet to be realized [15].

In terms of transport, the 1D nature of CNTs severely reduces the phase space for scattering, allowing CNTs to realize maximum possible bulk mobility of this material. The low scattering probability and high mobility are responsible for high "on" current (in excess of $1mA/\mu m$) in semiconductor CNT transistors. Furthermore, the chemical stability and perfection of the CNT structure suggests that the carrier mobility at high gate fields may not be affected by processing and roughness scattering as in the conventional semiconductor channel. Similarly in metallic CNTs, low scattering together

with the strong chemical bonding and extraordinary thermal conductivity allows them to withstand extremely high current densities (up to $\sim 10^9 A/cm^2$).

Electrostatics is improved in these devices as well. The fact that there are no dangling bond states at the surface of CNTs allows for a much wider choice of gate insulators beyond the conventional SiO_2. This improved gate control without any additional gate leakage becomes very important in the scaled devices with effective SiO_2 thickness below 1nm. Also, the strong 1D electron confinement and full depletion in the nanoscale diameter of the SWCNTs (typically $1-2nm$) should lead to a suppression of short-channel effects in transistor devices.

The combined impact of transport and electrostatic benefits together with the fact that semiconducting CNTs are, unlike silicon, direct-gap materials, suggests applications in opto-electronics as well.

As far as integration is concerned, semiconducting CNTs benefit from their band structure which gives essentially the same effective mass to electrons and holes. This should enable similar mobilities and performance in n-type and p-type transistors which is necessary for a complementary metal-oxide semiconductor (CMOS)-like technology. Finally, since CNTs can be both metallic and semiconducting, an all-nanotube electronics can be envisioned. In this case, metallic CNTs could act as high current carrying local interconnects while semiconductors would form the active devices. The most important appeal of this approach is an ability to fabricate one of the critical device dimensions (the CNT diameter) reproducibly using synthetic chemistry.

1.4 Fabrication and Performance of Carbon Nanotube Field-Effect Transistors

The first carbon nanotube field-effect transistors (CNT-FETs) were reported only a few short years after the initial discovery of the CNT [16, 17]. These early devices, shown schematically in Fig. 1.2a, were relatively simple in structure: Noble metal (gold or platinum) electrodes were lithographically patterned atop an oxide-coated, heavily doped silicon wafer, and a single-walled CNT was deposited atop the electrodes from solution. The metal electrodes served as the source and drain, and the CNT was the active channel. The doped substrate served as the gate electrode, separated from the nanotube channel by the thick ($\sim 100-200nm$) oxide layer. These devices displayed clear p-type transistor action, with gate voltage modulation of the drain current over several orders of magnitude. The devices displayed high parasitic resistance ($\gtrsim 1M\Omega$), low drive current, low transconductance, $g_m \sim 1nS$, high subthreshold slope, $S = [d(log_{10}I_d)/dV_g]^{-1} \sim 1V/decade$, and no current saturation. Due to the thick gate dielectric, these devices required large values of gate voltage (several volts) to turn on, making them unattractive for practical applications.

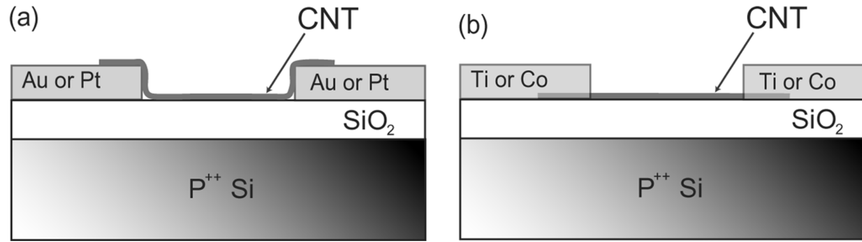

Fig. 1.2. **(a)** Schematic structure of first CNT-FETs, with CNT draped over metal electrodes. **(b)** "Improved" CNT-FET structure, with metal electrodes deposited upon the CNT, followed by thermal processing to improve contact. The substrate serves as the gate for both device structures, and it is separated from the CNT by a thick oxide layer

Following these initial CNT-FET results, advances in CNT-FET device structures and processing yielded improvements in their electrical characteristics. Rather than laying the nanotube down upon the source and drain electrodes, relying on weak van der Waals forces for contact, the CNTs were first deposited on the substrate, and the electrodes were patterned on top of the CNTs, as in Fig. 1.2b. In addition to Au, Ti and Co were used [18–20], with a thermal annealing step to improve the metal/nanotube contact. In the case of Ti, the thermal processing leads to the formation of TiC at the metal/nanotube interface [19], resulting in a significant reduction in the contact resistance – from several $M\Omega$ to $\sim 30k\Omega$. On-state currents $\sim 1\mu A$ were measured, with a transconductance of $\sim 0.3\mu S$, an improvement of more than 2 orders of magnitude relative to the van der Waals contacted devices. This CNT-FET device configuration can be found extensively in the literature (see, e.g., McEuen et al, [21]). More recently, it has been found that Pd forms low resistance contact to CNTs for p-type devices [12]. It is speculated [12] that Pd offers improved wettability of the CNT surface relative to other metals, as well as good Fermi level alignment relative to the nanotube band edge. This point will be explored further in the following section.

As mentioned above, early CNT-FETs were p-type in air, i.e., hole conductors. The role of the ambient on CNT-FET conduction will be discussed in detail below, however, it was found that n-type (i.e., electron) conduction could be achieved by doping from an alkali (electron donor) gas [22–24] or by thermal annealing in vacuum [19, 25]. In addition, it is possible to achieve an intermediate state, in which both electron and hole injection are allowed, resulting in ambipolar conduction [19, 25]. The ability to controllably fabricate both p-type and n-type CNT-FETs is critical to the formation of complementary metal-oxide-semiconductor (CMOS) logic circuits. Such CNT-FET circuits will be discussed later in this chapter.

Early experiments on CNT-FETs were built upon oxidized silicon wafers, with the substrate itself serving as the gate and a thermally grown oxide film,

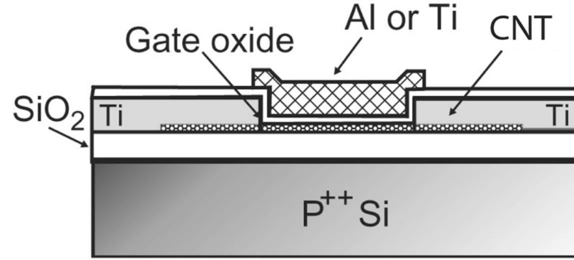

Fig. 1.3. Schematic cross-section of top-gate CNT-FET

typically $\sim 100nm$ or more thick, serving as the gate dielectric. The thick gate oxide required relatively high gate voltages ($\sim 10V$) to turn on the devices, and the use of the substrate as the gate implied that all CNT-FETs must be turned on and off together, precluding the implementation of complex circuits. A more advanced CNT-FET structure [26] is shown in Fig. 1.3. The device comprises a top-gate separated from the nanotube channel by a thin gate dielectric. The top-gate allows independent addressing of individual devices, making it more amenable to integration in complex circuits, while the thin gate dielectric improves the gate-channel (CNT) coupling, enabling low voltage operation. In addition, the reduction of the capacitance due to gate-to-source and gate-to-drain overlap suggests that such a device structure would be appropriate for high frequency operation. Such a CNT-FET can also be switched using the conductive substrate as a bottom gate, allowing for direct comparison between top and bottom gate operation. Comparison of the output characteristics for top and bottom gate operation of the device in Fig. 1.3 are shown in Fig. 1.4a and 1.4b, respectively. Operating the device with the top-gate yields distinctly superior performance relative to bottom gate operation, with a lower threshold voltage ($-0.5V$ vs.$-12V$) and higher transconductance ($g_m = 3.25\mu S$ vs. $0.1\mu S$). Figure 1.4c shows superior subthreshold behavior for top-gate operation with an improvement in subthreshold slope of more than a factor of 10 ($130mV/decade$ vs. $2V/decade$).

In order to gauge whether or not CNT-FETs have potential for future nanoelectronic applications, it is important to compare their electrical performance to those of advanced silicon devices. Wind et al. [26] demonstrated that although the device structure is far from optimized, the electrical characteristics, such as the "on current" and the transconductance, g_m, of the device shown in Fig. 1.3 exceeds those of state-of-the-art silicon MOSFETs. Further enhancements to CNT-FET structures, such as the use of high dielectric constant gate insulators [27, 28], and additional improvements in the metal/nanotube contact resistance at the source and drain [12] have lead directly to improved CNT-FET performance. Such improvements are not restricted to p-type CNT-FETs. Fig. 1.5 shows the transfer characteristics of

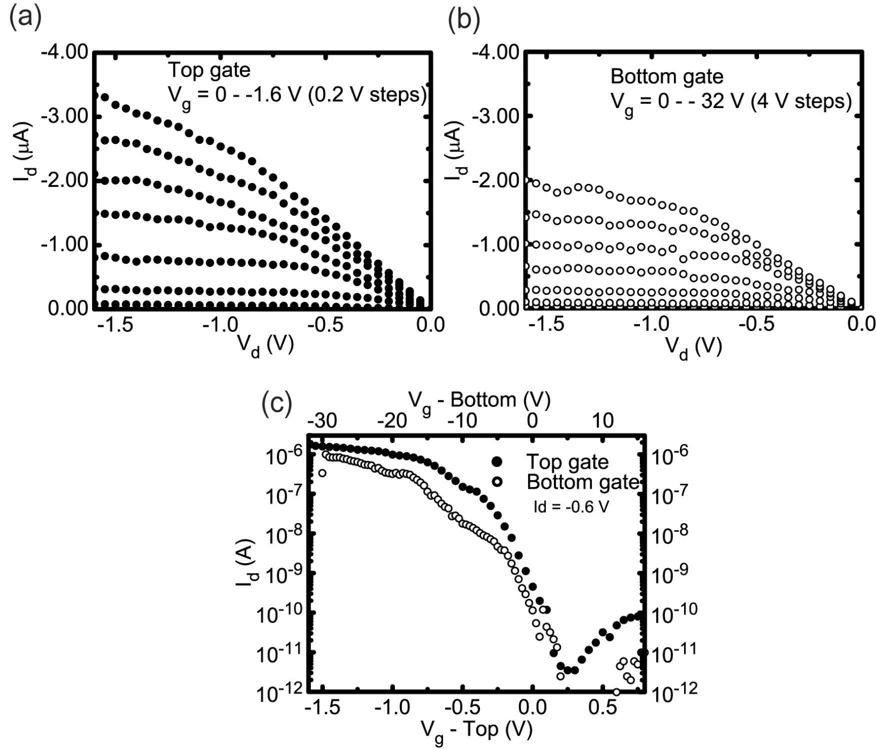

Fig. 1.4. Electrical characteristics of the CNT-FET shown in Fig. 3 for both top-gate and bottom-gate operation. The oxide thicknesses for the top gate and the bottom gate are 15 nm and 120 nm, respectively. **(a)** and **(b)** Output characteristics. **(c)** Transfer charactersitics for top- and bottom-gate operation

an n-type CNT-FET with a thin ($5nm$) SiO_2 gate dielectric fabricated by potassium doping of a p-type device [29].

It is not sufficient to fabricate individual CNT-FETs. Future applications will require vast numbers of devices on a single substrate. In an effort to test the parallel fabrication of many CNT-FETs, Collins et al. [30] deposited mixtures of individual and ropes of CNTs upon an oxidized silicon wafer and formed a regular array of source, drain and gate electrodes. Although the deposited mixture of nanotubes contained random mixtures of semiconducting and metallic CNTs, functional FETs could be formed by selectively destroying the metallic nanotubes in a controlled manner via application of a sufficiently high current. The semiconducting tubes were preserved by using the gate electrode to deplete them of carriers during the destruction of the metallic tubes, leaving behind a large array of functional CNT-FETs [30]. In another approach, CNT-FETs were fabricated upon an existing silicon NMOS decoder circuit using CVD growth from metal catalysts located on the silicon

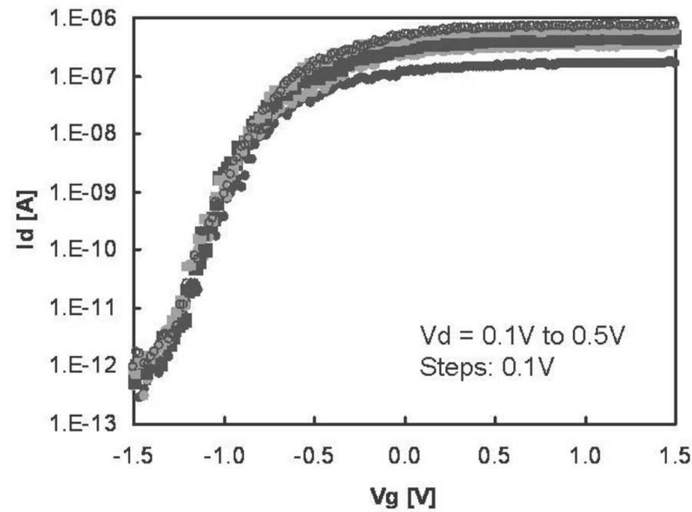

Fig. 1.5. Transfer characteristics of an n-type CNT-FET on 5 nm thick gate oxide (from Ref. [29])

devices [31]. The decoder was used for rapid electrical characterization of the CNT-FETs.

CNTs are also being explored for low cost, low performance applications, such as thin film transistors (TFTs). Snow et al. [32] formed large area transistors by depositing random arrays of nanotubes between metal electrodes. They found that conduction between the electrodes could proceed via percolation through the network of CNTs. Their devices had field-effect mobilities $\sim 10cm^2/V-s$, which is significantly higher than TFTs made from amorphous silicon [32]. The off-state current in these devices is limited by the presence of metallic nanotubes in the percolation network. In order for CNT-based TFTs to be practical, transport through these metallic tubes must be reduced.

1.5 Carbon Nanotube Transistor Operation in Terms of a Schottky Barrier Model

While the performance of CNT-FETs shows a great deal of promise, further improvements and optimization, especially in scaled devices requires a detailed understanding of the switching mechanism. So far we have made an implicit assumption that the conventional or bulk switching of silicon devices is applicable to CNT-FETs [33]. However, this notion may not be entirely correct in all situations, since in general the charge transfer must take place at the metal-nanotube interface leading to band-bending in CNTs and the

creation of a Schottky barrier (SB) [34]. While this barrier is present at the metal-semiconductor contact, its height is dependent on a number of material parameters such as workfunction difference, as well as the interface quality. For this reason, significant amount of effort has been and continues to be made in order to search for the right material and process combination that yields a barrier free junction in CNT devices [12, 35]. Such CNT-FETs would show minimal effect of the SB on transport and consequently approach a more traditional bulk switching, CMOS-like behavior. However, evidence for rather high Schottky barriers which affects the performance of CNT-FETs in most device geometries is still clearly present. For example, a CNT-FET with titanium-carbide contacts show equal hole and electron currents depending on the sign of the applied gate bias, V_g, so called ambipolar conduction [19]. This suggests the existence of two barriers, one for electrons and one for holes, of approximately equal height implying that each must be about half the bandgap ($E_{gap}/2 \sim 300meV$). Applying conventional semiconductor analysis indeed yields similar thermal activation barriers but on the order of $10meV$ [19]. This finding suggested that thermionic contribution alone can not account for the observed current levels, which is supported by modeling results showing that Schottky barriers in 1D are much thinner than their planar analogues [14]. Consequently, carrier tunneling through these thin barriers becomes dominant conduction mechanism and cannot be neglected when quantifying the barrier height [36].

Similar conclusions can be drawn from attempting to understand the sub-threshold behavior of CNT-FETs, in particular as a function of gate oxide thickness. The switching of a MOSFET is described by the inverse sub-threshold slope, S, defined in the previous section, is approximated by $S \simeq k_B T/q \cdot ln(10) \cdot (1 + C_D/C_g)$where C_D and C_g are the depletion and gate capacitance, respectively. In the case of a fully depleted device, C_D is zero and, therefore, S depends only on the temperature, having a value of $65mV/decade$ at room temperature. The original CNT-FETs with thick gate oxides in back-gated geometry had unexpectedly high S values of approximately $1,000mV/decade$. Moreover, similar high values of S are observed for both charge carriers types in unipolar and ambipolar devices, eliminating the influence of oxide traps as a possible explanation. On the other hand, when devices are fabricated using thinner oxides, such as the top-gated CNT-FET in Fig. 1.3, the value of S dropped significantly into the range of $100 - 150mV/decade$ [26]. Such a dependence of S is not consistent with bulk switching mechanism which should give $65mV/decade$ in the long channel limit. Instead, this unorthodox scaling of the subthreshold slope with oxide thickness is compatible with existence of sizeable Schottky barriers at the metal/CNT junctions, and theoretical modeling showed that the gate field impact on at this junction is responsible for the improvement in S observed [37, 38].

Further evidence of the presence of Schottky barriers in the CNT-FET devices is found in local gating experiments. In one study, the on-current in CNT-FETs is shown to increase significantly by an application of a local potential from a metal coated scanning probe tip only at the positions above the metal/CNT junction [39]. Similarly, the impact of Schottky barriers in the sub-threshold characteristics of the CNT-FET is clearly observed in transistors with multiple, lithographically patterned top-gates [10]. In this case, local gates over the metal/CNT junction are used to electrostatically thin the Schottky barriers and reduce the S value closer to that of the bulk switching device [10] (see Fig. 1.10).

More recently, different groups of researchers have identified material combinations that decrease the barrier height and improve the on-state performance of CNT-FETs. For example, by using larger diameter (smaller bandgap) CNTs, in combination with the metal of the right workfunction one can hope to reduce the barrier for one charge carrier type. This lowering and effective removal of the barrier is seen for CNTs with diameter, $d_{CNT} > 2nm$ and Pd electrodes. In that case, nearly ohmic p-type CNT-FETs are produced, while the barrier still remains for the same devices when operated as n-type transistors [12]. Similarly, even the p-type CNT-FETs with Pd electrodes show significant barriers if d_{CNT} is well below $2nm$. Other groups have also reported nearly ohmic contacts for similar or larger d_{CNT} nanotubes and Au/Cr or pure Au electrode combinations [13, 40]. In addition, the effect of the Schottky barriers can be reduced by studying very long (in excess of $100\mu m$) channel CNT-FETs, where the bulk nanotube resistance is mainly responsible for the device performance [40]. This and other dependences of the device performance on the material parameters of the CNT will be discussed in the next section.

1.6 The Role of Nanotube Diameter and Gate Oxide Thickness

The electronic properties of CNTs are strongly dependent upon the tube diameter, d_{CNT}, and chirality (given by the chiral indices m and n), as described earlier in this chapter. The CNT bandgap, E_{gap}, is inversely proportional to d_{CNT}, as is the effective mass, m^*, for electrons and holes. Thus, at a given temperature, large diameter CNTs will have a larger free carrier concentration than smaller diameter nanotubes, and they will have a lower effective mass. In addition, because of the smaller E_{gap} of large diameter CNTs, the band lineup at the metal/nanotube interface will likely result in lower Schottky barriers at the source and drain. Tunneling through these barriers will be easier as well because of the smaller m^*. As a result, CNT-FETs comprising large diameter tubes should be capable of higher I_{ON} than those with smaller d_{CNT}. This is borne out in the literature, as CNT-FETs carrying large on currents are generally fabricated with tubes grown by CVD [12, 41],

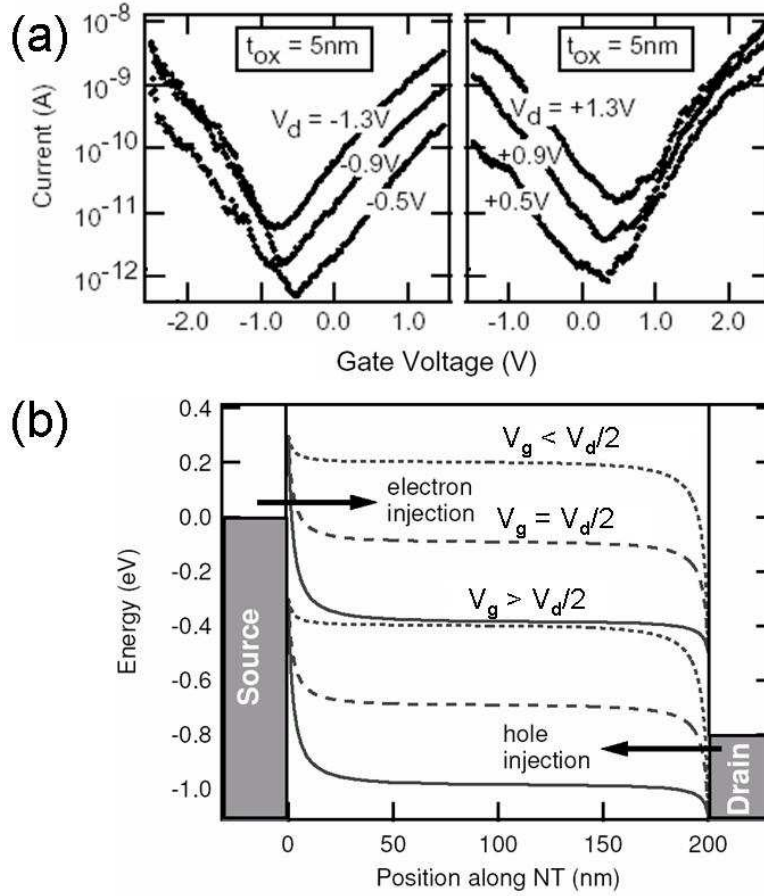

Fig. 1.6. (a) Transfer characteristics of ambipolar CNT-FET with ultrathin gate oxide. **(b)** Band bending situation for (a) (from Ref. [73])

which typically have larger diameters ($\sim 2-4nm$) than those grown by laser ablation [42] or HiPCO [43] techniques ($\sim 0.8 - 1.5nm$). Certainly, a high on-state current is a most desirable property and is a requirement for many device applications, however, a low off-state current is just as important, particularly for low power applications. I_{ON}/I_{OFF} ratios of at least $10^4 - 10^5$ are the norm for advance silicon technology [44]. In the case of CNT-FETs, those factors that tend to lead to higher on-state currents (smaller E_{gap}, lower Schottky barriers, small m^*) also make it difficult to achieve acceptably low I_{OFF}. This problem is exacerbated for the case of extremely scaled gate insulators. Reducing the gate dielectric thickness while maintaining a constant V_{gs} results in further thinning of already-thin Schottky barriers at both the source and the drain electrodes, increasing the probability of drain

current leakage. Fig. 1.6 illustrates this effect for an ambipolar CNT-FET with ultrathin gate oxide (the transfer characteristics are shown in Fig. 1.6a, while the theoretical band bending situation [45] is shown in Fig. 1.6b.) This drain leakage current increases exponentially with increasing drain voltage, resulting in a reduced I_{ON}/I_{OFF} ratio. It may be possible to alleviate this problem by designing an asymmetric CNT-FET in which the gate field at the source and drain are different, resulting in different injections rates for electrons and holes. Such an asymmetric device, with a narrow trench designed below the CNT in the vicinity of the drain electrode, is shown in Fig. 1.7 [46]. Incorporating such a feature in a CNT-FET may be an undesirable

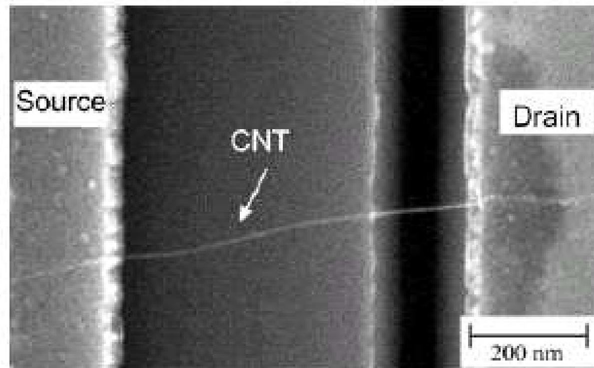

Fig. 1.7. CNT-FET with asymmetric trenches near the drain designed to decouple Schottky barriers effects from the CNT bulk (from Ref. [46])

complication, and it may be unfeasible for very thin gate dielectrics. Thus, practical considerations dictate that the appropriate choice of CNT diameter and gate dielectric thickness be a trade-off between achieving a high I_{ON} at the highest tolerable I_{OFF}.

1.7 Environmental Influences on the Performance of CNT-FETs

The effect of ambient air on the performance and functionality of CNT-FETs can be also understood within the framework of the Schottky barrier model of conduction. In particular, this model helps clarify and separate the effects due to the bulk of the nanotube channel from those arising from the effects at the contact between the metal electrode and the nanotube.

As has already been discussed in the introduction, the original back-gated CNT-FETs operating in air function as p-type transistors without any explicit doping of the CNT [16, 17]. Similar CNT devices operated in

two-terminal configuration (without the backgate) showed an increase in the electrical resistance and sign change of the Seebeck coefficient upon removal of air [30]. This is not surprising since in most cases nanotubes in these devices are open to air and no effort is made to protect them from the environmental influences. Further study of specific gases identified that most of this effect was associated with oxygen, and thus a proposal was made that the effect is due to electron transfer between CNTs and atmospheric O_2; in particular that CNTs are hole doped in the ambient and n-doped or intrinsic in vacuum.

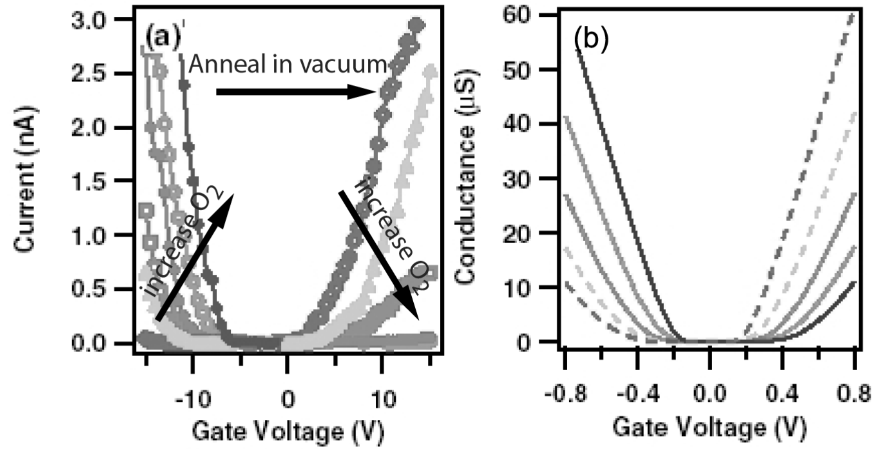

Fig. 1.8. Effect of environment on carbon nanotube FETs. **(a)** A Au-contacted p-FET is converted to n-FET by annealing in vacuum. Slow reintroduction of oxygen, as denoted by arrows, simultaneously suppresses electron conduction at positive V_g and increases the hole conduction at negative V_g without changing the threshold voltage of the transistor. **(b)** Simulations assuming only the change in metal workfunction with change in oxygen pressure show qualitative agreement with data (from Refs. [25, 38])

These results were extended by investigation of the impact of gases on three-terminal CNT-FETs. As shown in Fig. 1.8a, a CNT-FET which has been annealed in vacuum behaves as an n-type transistor [25]. The slow re-introduction of dry O_2 shows that the original, p-type character can be recovered at atmospheric pressure with intermediate stages of ambipolar conduction also readily observable. This behavior is consistent with the previous reports that p-type character of CNT-FETs is a result of the interaction with O_2, but it also provides additional information which together with other experiments [47], and theoretical modeling [38] helps clarify the nature of this interaction. In particular, it is apparent that this treatment has no effect on the threshold voltage, which shifts quite significantly when nanotubes are doped by potassium, which is a well-established dopant.

Thus, the joint conclusion of these studies is that the effect of O_2, rather than doping is that it adsorbs at the metal/CNT junction and modifies the Schottky barriers that control the switching of the CNT-FET. As we have already discussed earlier in this chapter, the bonding of a CNT to a metal electrode results in charge transfer and creation of the Schottky barrier at the CNT/metal interface. The actual band line-up and charge-transfer may be strongly affected by the co-adsorption of other species such as gaseous oxygen at the junction. The role of the adsorbates is to locally change the surface potential (local work function), or directly interact with the metal/CNT interface [38, 47]. Modeling results in Fig. 1.8b of the surface potential change with oxygen presence result in curves without any threshold shift as seen in the experiment [38]. In fact, direct observation of this modification has been achieved by scanning probe techniques [47]. Figure 1.9 shows scanning Kelvin probe images of a few CNTs dispersed on a gold surface in the ambient (b) and in vacuum following a mild anneal (c). (The contrast between CNTs and the Au substrate changes as the sample is cycled between air and vacuum indicating a reversal in the charge transfer direction between CNT and Au, and in turn facilitating injections of holes and electrons, respectively into a CNT device.) These findings may also have technological implications, as the sensitivity of the Schottky barriers to other co-adsorbed species may be applicable for engineering of the CNT-FET characteristics [47].

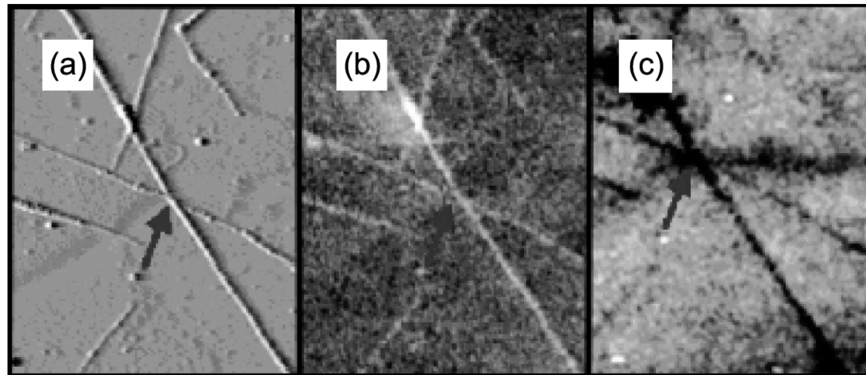

Fig. 1.9. In situ Scanning Kelvin probe microscopy (SKPM) of CNTs on gold in controlled environment. **(a)** Atomic force microscope image of CNTs on flame annealed (111) Au. **(b)** - **(c)** SKPM of the same area in air and ultra-high vacuum (UHV), respectively. Nanotubes appear brighter which implies a lower vacuum level than gold in air and vice versa in UHV. Arrows indicate same position in all three images (from Ref. [47])

1.8 Scaling of CNT-FETs

The incredible growth of the silicon microelectronics industry has been based upon the ability to scale transistor features to smaller and smaller dimensions. Transistor scaling rules are well understood and are based upon straighforward electrostatic considerations [34]. Because the CNT-FET geometry differs from that of a planar silicon FET, it would be expected to follow different scaling rules. For example, in the case of a planar Si MOSFET, the current is inversely proportional to the gate dielectric thickness. However, the geometry of a CNT-FET is quite different; it corresponds more closely to that of a small conducting cylinder and a large planar electrode (the gate). In this case, for bulk switching, simple electrostatics would dictate a weak inverse logarithmic dependence of the current on insulator thickness [20]. Furthermore, as mentioned above, the basic switching in most CNT-FETs measured to date involves the gate field-induced modulation of Schottky barriers at the source and drain electrodes. This mechanism can be extremely sensitive to the precise device geometry, i.e., CNT-FET structures which produce a high electric field at the metal/nanotube junction produce the most effective switching [48]. Heinze et al. [48] found unexpected geometry-dependent vertical scaling laws for the subthreshold slope and transconductance for back-gated Schottky barrier CNT-FETs with variable gate oxide thickness.

The lateral scaling of CNT-FETs is affected by the fact that at low excitations, the elastic mean free path, λ_{el}, is relatively long, $\gtrsim 1\mu m$. Thus, for relevant device channel lengths, transport is essentially ballistic. Using a segmented gate device shown in Fig. 1.10a to decouple switching in the CNT bulk from Schottky barrier switching, Wind et al. [10] observed length-independent transport in the bulk regime (Fig. 1.10b), providing evidence for ballistic transport in CNT-FETs. Javey et al. [12] also reported evidence for ballistic transport based on measured on-state conductance approaching G_0. Thus, for channel lengths of a few hundred nanometers or less, length scaling does not apply to CNT-FETs, at least for *dc* operation (*ac* transport will be affected by time-of-flight effects). For much longer nanotubes, scattering is indeed evident [40], although these devices still exhibit unusually high mobilities ($> 100,000 cm^2/V - sec$).

1.9 Prototype Carbon Nanotube Circuits

The promising characteristics of individual CNT-FETs have lead to initial attempts at integration of these devices into useful structures of several CNT-FETs that can perform a logic operation, function as memories [49] or sensors [50]. In the following, we limit our discussion to advances in logic circuitry.

The nanotube logic gates have been, in most cases, based on a complementary technology analogous to silicon CMOS, which is important as it may ease integration of CNTs onto this well established technology. The

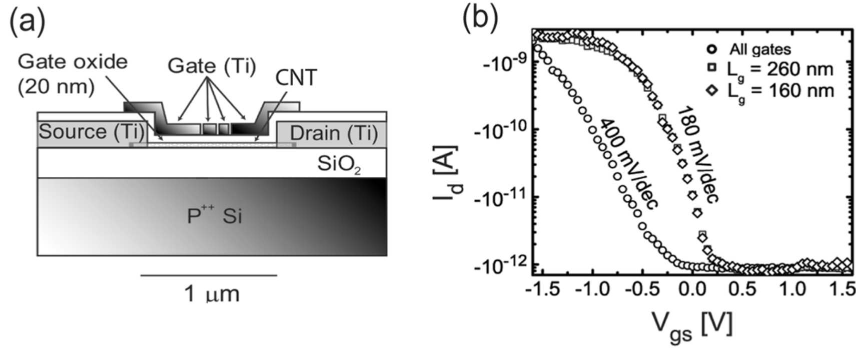

Fig. 1.10. (a) Schematic cross-section of segmented top-gate CNT-FET. **(b)** Transfer characteristics showing the difference between Schottky barrier modulation achieved by operating all gate segments together (open circles) and bulk switching achieved by independent operation of different combinations of interior gate segments (open squares and diamonds)

first complementary (CMOS-like) logic gates were reported by Derycke et al. [23] In this work, two different techniques were used to produce n-type devices for complementary logic – resulting in multiple transistor logic gates fabricated from adjoining nanotubes, or on the same tube. Inter-nanotube voltage inverter ("NOT" gate) is created by combining two CNT-FETs: a p-type device in the ambient and a vacuum annealed n-type transistor. A more compact and integrated approach uses potassium doping to convert one of two CNT-FETs on the same nanotube to n-type. The masking of the other transistor which remains p-type is accomplished by photoresist. The completed device, an intra-nanotube CMOS inverter is shown in Fig. 1.11. The circuit shown has a voltage gain of about 2, suggesting that integration, without signal degradation, of many devices along a single nanotube can be accomplished. It is important to note that these initial and indeed all other logic circuits to date have been built using unoptimized CNT-FETs, which suggests that their performance will only improve with further advances in design and fabrication of individual devices as well as development of novel integration schemes.

Shortly thereafter, Bachtold et al. [51] used p-type CNT-FETs along with resistors to build prototype logic gates based on an older transistor-resistor scheme. They went a step further in complexity and wired three such inverter gates to form a ring oscillator. Unfortunately, the large parasitics severely degraded the performance of the circuit which oscillated at only about 5 Hz. Later Javey and co-workers [52] used another scheme for converting into n-type CNT-FETs to wire up CMOS inverters with gains in excess of 10 and CMOS ring oscillators with frequencies in the 100 Hz range.

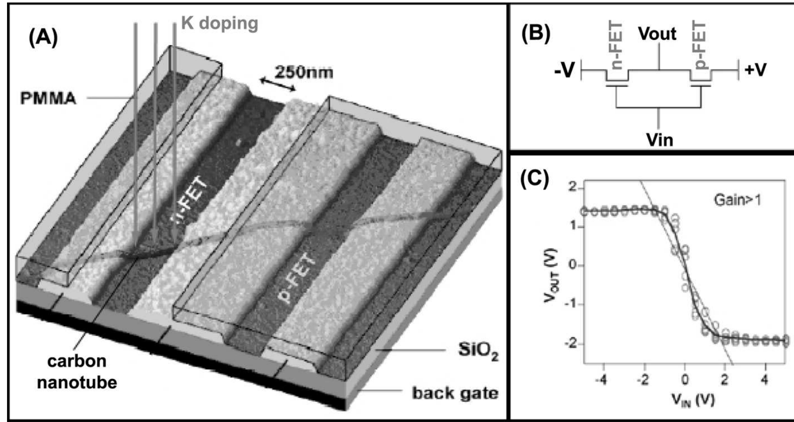

Fig. 1.11. (a) Logical NOT gate fabricated on a individual CNT-FET. **(a)** Sample geometry showing an individual semiconducting nanotube, laying across three electrodes. One of the two FETs is protected by PMMA polymer and remains p-type. The other is exposed to potassium doping and is converted to n-type. **(b)** Schematic of the circuit for the voltage inverter. Common backgate is used as V_{in}, common contact is used as V_{out}, while other two contacts have $\pm V$ applied. **(c)** Inverter characteristics showing gain larger than 1 (solid black line) (from Ref. [23])

However, these reported frequencies are well below the expected *ac* response of CNT-FETs which is difficult to assess because of the relatively small current signals in these devices. Most recently, the non-linear current-voltage characteristics of CNT-FETs were used to demonstrate that CNT-FETs *dc* characteristics are not affected by *ac* fields at least up to 0.5 GHz [53].

1.10 Optoelectronic Properties of Carbon Nanotubes

Semiconducting nanotubes, unlike silicon, have a direct band-gap in momentum space [1]. As a result, no momentum transfer is needed to induce interband transitions and direct light absorption and emission is possible. At the same time, the 1D confinement of the electron (e) and hole (h) is expected to lead to a strong e-h interaction leading to the formation of 1D excitons [5, 54–57]. Early optical absorption studies of CNTs involved bulk mixtures of metallic and semiconducting CNTs and showed broad spectral features [58, 59]. It was later found that CNTs can be dispersed effectively in a liquid medium using surfactants. Semiconducting CNTs encapsulated inside micelles showed relatively narrow absorption and photoluminescence excitation and emission spectra [60–62]. In addition to photoluminescence from CNTs in micelles in the liquid state, laser-excited photoluminescence from CNTs in micelles deposited on solid substrates [63], as well as spectra from suspended CNTs have been reported [64]. As an analytical tool, the

photoluminescence studies of dispersed CNTs have proven to be extremely valuable because, in conjunction with Raman experiments, they permit the identification of the(n, m) indices of the CNTs in a given sample.

Most experimental papers have discussed the excitations of CNTs in terms of band-to-band transitions, i.e. transitions between van Hove singularities, and have used tight binding theory (TBT) to interpret the spectra. However, a single-particle description of the excited CNT states neglects electron–electron and electron–hole interactions, which should be particularly strong in a 1D system [5,54]. The latter interaction is expected to bind the photoexcited electron and hole to form Wannier-like excitons [5,54–57]. Indeed, first-principles electronic structure calculations that are based on a many-body Green's function approach in which both the quasiparticle (single-particle) excitation spectrum and the optical (electron-hole excitation) spectrum were computed, predict the formation of strongly bound CNT excitons. In fact, exciton formation with a binding energy approaching $100meV$ was predicted even in the case of the small metallic $(3, 3)$ CNT [56]. For the semiconducting $(8, 0)$ CNT a binding energy of $\sim 1eV$ was obtained. The LDA value for the band-gap of this CNT was $0.6eV$ at the Γ-point, but after quasiparticle corrections opened up to $1.75eV$ [56]. While expected to be quite accurate such calculations are very laborious and thus are limited to a few small systems. For this reason Perebeinos et al. [57] recently performed approximate calculations based on TB wavefunctions, but included both the direct and exchange $e - h$ interactions using the Bethe-Salpeter equation [65]. These calculations allowed them to derive general scaling rules for the properties of CNT excitons as a function of their diameter/chirality and the dielectric constant of the environment. It was found that the exciton binding energy, E_b, scales with the CNT radius R, effective mass m, and dielectric constant ε as [57]:

$$E_b = A_b(R/a_B)^{\alpha-2} \cdot (m/m_e)^{\alpha-1}\varepsilon^{-\alpha}. \tag{1.1}$$

In equation 1.1, a_B is the Bohr radius, m_e is the free electron mass, while A_b and α are fitting parameters, with $A_b = 24.1eV$ and $\alpha = 1.4$. Most importantly, they found a strong transfer of intensity from the interband transition to the exciton. When the binding is large, all absorption intensity is concentrated in the exciton (see Fig. 1.12) [57]. Recent time-resolved studies of the excited states of CNTs support the exciton picture on the basis of the observation of strong transitions where forbidden interband transitions are expected, and on the measurement of polarization memory in photo-induced absorption and photo-bleaching bands that lasts on a relatively long (ps) time scale [66]. Other evidence comes from the observation of vibronic side bands in the photoconductivity spectra of single CNTs (see discussion below) [67]. The lineshapes and the relative intensities of the zero-phonon line and vibronic side-band can be accounted for only within the excitonic picture [57].

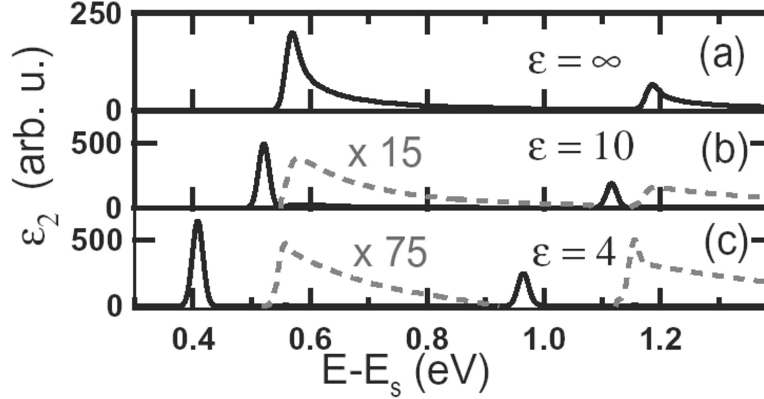

Fig. 1.12. Computed absorption spectra ε_2 of a $(19, 0)$ carbon nanotube in different dielectrics. **(a)** $\varepsilon = \infty$, equivalent to no electron-hole interaction. **(b)** $\varepsilon = 10$, and $\varepsilon = 4$. E_s is the unknown self-energy shift. (from Ref. [57])

For optoelectronic applications, solid-state, electrically driven CNT light-emitting devices and light detectors are desirable. Photogenerated currents from CNTs have been reported by several groups [68–70]. Early studies involved bundles of semiconducting and metallic nanotubes. Recently, however, photocurrents and photovoltage from individual CNTs in ambipolar and unipolar CNT-FETs were also reported [71]. As shown in Fig. 1.13, scanning the laser in the range of the second exciton state of a laser-ablation CNT produces a well-defined peak in the photocurrent spectra at $1.35eV$ and a side band $\sim 180meV$ higher energy. The peak corresponds to the energy of the zero phonon line of the second exciton, while the side band is due to a C–C stretching optical mode of the CNT [1]. The estimated quantum yield of photon to e–h pair conversion in the ambipolar CNT-FETs is $\sim 10\%$ [71]. Thus, CNT-FETs can act as efficient photodetectors with the added capability of polarization detection.

Ambipolar CNT-FETs can be used to produce a single gate-controlled light source [72]. In the case of Schottky barrier ambipolar devices with a symmetric source and drain structure, it was shown that about equal currents of electrons and holes are injected from opposite ends of the CNT when $V_g = V_d/2$ [73]. The electrons and holes are confined by the 1D CNT structure; where they meet, a fraction of them, determined by momentum and spin selection rules and other factors, may radiatively recombine. Indeed, IR emission was observed from ambipolar CNT-FETs [72]. This emission was polarized along the CNT axis and, most importantly, the emission intensity was found, as predicted, to be the highest when $V_g = V_d/2$. The peaks of the electroluminescence emission spectra [74], were in accord with the expected band-gaps of the CNTs used in the experiment. However, the

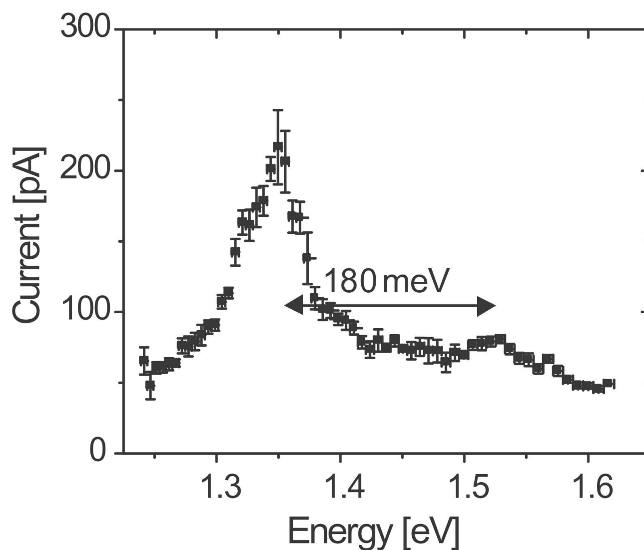

Fig. 1.13. Photoconductivity spectrum of a single semiconducting nanotube. The main peak at $\sim 1.35eV$ corresponds to the zero-phonon line of the second allowed electronic transition of the nanotube, while the side peak at $\sim 180meV$ higher energy involves the simultaneous excitation of one quantum of a C-C stretch optical phonon. From Ref. [67])

electroluminescence peak shape was found to depend on the length of the CNT channel. Long CNTs ($\gtrsim 5\mu m$) gave narrow, nearly symmetric peaks; an example is shown in Fig. 14. Short CNTs ($\sim 200 - 300nm$), on the other hand, produced broad asymmetric spectra [74]. These observations were interpreted in terms of a complete or a partial relaxation of the hot carriers during their residence time in the long, or short CNTs channels, respectively. From the broad lineshapes the energy distributions of the carriers were deduced and interpreted in terms of fast relaxation through coupling with optical phonons followed by a slower relaxation via the acoustic phonons. Very recent spatially-resolved studies of the light emission from CNT-FETs involving very long (e.g., $\sim 50\mu m$) CNTs, as a function of the applied gate and drain biases, have provided unique insights on electrical transport processes in a CNT [75]. Unlike the case of LEDs where chemical doping defines the location of the light emission, the ambipolar CNTs are undoped and the position of the light emission is controlled by the gate as shown in Fig. 1.15. The emitting spot gives the location where the electron- and hole-current meet inside the CNT, while its shape allows the determination of the e-h recombination lengths. Local sources of e-h pair creation at high fields such as Zener tunneling and hysteresis effects can also be visualized [75].

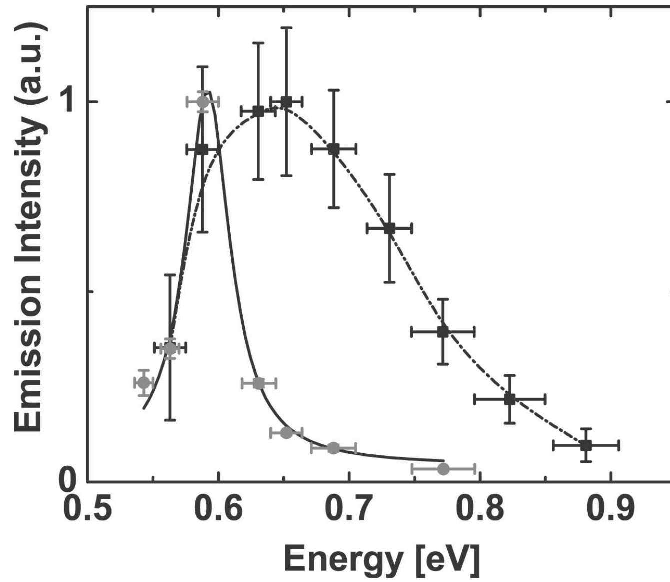

Fig. 1.14. Electroluminescence from a long ($\sim 50\mu m$) carbon nanotube field effect transistor. The emission spot can be translated along the axis of the nanotube by varying the gate bias under constant current ($18\mu A$) conditions. (From Ref. [71])

1.11 Summary

In this chapter, we have discussed the properties of CNTs that make them ideally suited for electronic and optoelectronic applications. Already CNT-FET transistors that outperform their silicon counterparts have been demonstrated. Moreover, the CNT-FET, depending on the biasing conditions, can not only be as an electrical switch, but also as a novel light source and a light detector. Finally, CNTs provide an ideal model system to study the electrical transport properties of 1D nanostructures and molecules.

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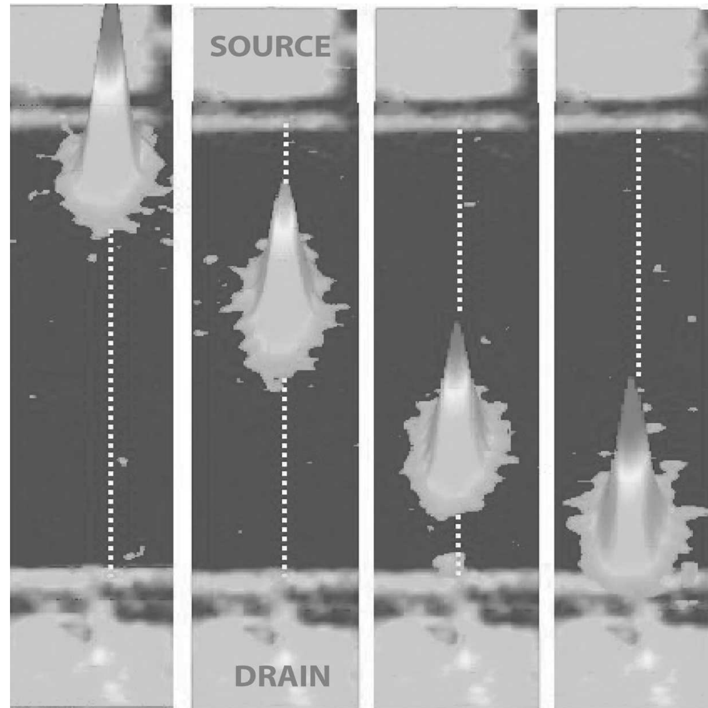

Fig. 1.15. Electroluminescence (i.e. emission due to radiative e-h recombination) spectra of a short ($\sim$ $300nm$) and a long ($\sim$ $50\mu m$) nanotube incorporated as channels of field-effect transistors. (From Ref. [75])

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